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By

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THEME

Contribution to the FPGA implementation of an embedded system for ECG signals

Defended on 19/11/2022 (1444 / ربيع الثاني / 25) before the jury composed of:

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بِسْمِ اللّٰهِ الرَّحْمٰنِ الرَّحِيْمِ ۝
اَلْحَمْدُ لِلّٰهِ رَبِّ الْعٰلَمِيْنَ ۝١ الرَّحْمٰنِ الرَّحِيْمِ ۝٢
مٰلِكِ يَوْمِ الدِّيْنِ ۝٣ اِيَّاكَ نَعْبُدُ وَاِيَّاكَ نَسْتَعِيْنُ ۝٤
اِهْدِنَا الصِّرَاطَ الْمُسْتَقِيْمَ ۝٥ صِرَاطَ الَّذِيْنَ اَنْعَمْتَ
عَلَيْهِمْ ۙ غَيْرِ الْمَغْضُوْبِ عَلَيْهِمْ وَلَا الضَّآلِّيْنَ ۝٦

Praise be to Allah alone, He has no partner

My Prayers on Muhammad, the Prophet of Allah

To my dear parents and my wife's parents

To my dear wife and daughter (Ilef)

To my family

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Acronyms

ADC/DAC Analog to Digital Convert/Digital to Analog Convert

AFDW Alexander Fractional Differential Window

AICF Adaptive Impulse Correlated Filter

ANN Artificial Neural Networks

ANOVA ANalysis Of VAriance

AP Action Potential

AP All Programmable

ARF Adaptive Recurrent Filter

ARP Absolute Refractory Period

ASIP Application-Specific Instruction Processors

ASSP Application Specific Standard Product

ASSP Application-Specific System Processor

AV Atrio-ventricular node

BC Best Configuration

BLW Baseline Wander

BSF Band Stop Filter

BSPM Body Surface Potential Mapping

CISC Complex Instruction Set Computer

CVD Cardiovascular Diseases

DAD Delayed After Depolarization

DMA Direct Memory Access

DSP Digital Signal Processing

DWT Discrete Wavelet Transform

DWT Discrete Wavelet Transforms

EAD Early After Depolarization

ECG Electrocardiogram

EDK Embedded Design Kit

EMD Empirical Mode Decomposition

EMG Electromyography

FDA Filter Design and Analysis

FFT Fast Fourier Transform

FIR Finite Impulse Response

FPGA Field Programmable Gate Array

GPIO General Purpose Input/Output

HPF High Pass Filter

HRT Heart Rate Turbulence

HRV Heart Rate Variability

ICA Independent Component Analysis

IDWT Inverse Discrete Wavelet Transform

IIR Infinite Impulse Response

INA Instrumentation Amplifier

ISCS Intra-ventricular Special Conduction System

ISE Integrated Software Environment

LMS Least Mean Square

LPF Low Pass Filter

LUT Lookup Tables

MADALINE Multiple ADAptive LINear Element

MSE Mean Square Error

NLMS Normalized Least Mean Square

NRF Noise Reduction Factors

PCA Principal Component Analysis

PLI Power Line Interference

PNR Percentage Noise Retention Ratio

PS Processing System

PTB Physikalisch-Technische Bundesanstalt

RISC Reduced Instruction Set Computer

RRP Relative Refractory Period

RTOS Real-Time Operating System

SA Sino-atrial node

SCD Sudden Cardiac Death

SCI Serial Communication Interfaces

SCS Special Conduction System

SDLMS Sign Data Least Mean Square

SELMS Sign Error Least Mean Square

SNR Signal to Noise Ratio

SoC System on Chip

SoPC System on Programmable Chip

SSLMS Sign-Sign Least Mean Square

STFT Short-Time Fourier Transform

SVM Support Vector Machine

TRP Total Refractory Period

TSAF Time-Sequenced Adaptive Filter

USB Universal Serial Bus

VCG Vector cardiogram

VHDL VHSIC Hardware Description Language

VLSI Very Large Scale Integration

WGN White Gaussian Noise

WT Wavelet Transforms

XSG Xilinx System Generator

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الملخص

تحتوي هذه الرسالة على دراسة شاملة لإشارة مخطط كهربية القلب ، حيث تتضمن عدة فصول مترابطة تحتوي على سلسلة من المعلومات عن قلب الإنسان. ركزت الدراسة على إزالة الضوضاء باستخدام طريقة مرشح متسلسل لثلاثة مرشحات FIR. في المقالة الأولى ، تتضمن الطريقة دراسة تنقية إشارة ECG عن طريق اختيار النوافذ جنبًا إلى جنب مع أجزاء المرشح المتتالية. تحتوي المقالة الثانية على طريقة دراسة ترشيح إشارة ECG عن طريق تحليل التباين الناتج عن تبادل مواضع مرشحات الفلتر المتتالي بواسطة ANOVA. أسفرت كلتا الطريقتين عن نتائج مبهرة مقارنة بالعمل الأخير السابق. وهكذا توصلنا إلى أن هاتين الطريقتين أعطتا نتائج متكافئة بغض النظر عن الطريقة المستخدمة . لقد قدمنا أيضًا امتدادًا للمساهمة في تضمين FPGA من خلال تسخير Matlab Simulink SG، المتصل بـ XILINX ZedBoard، حيث تلقت هذه المساهمة نتائج ذات أهمية كبيرة في مجال الأنظمة المحمولة.

كلمات مفتاحية : ECG ، التتالي ، FIR، ضوضاء ، SNR، MSE، النافذة ، قاعدة بيانات PTB ، التباين ، التشخيص.

Abstract

This thesis contains a comprehensive study of the electrocardiogram signal, as it includes several interrelated chapters containing a series of information on the human heart. The study focused on noise removal using a sequential filter method of three FIR filters. In the first article, the method involves the study of electrocardiogram signal purification by selecting windows combined with successive filter portions. The second article contains the method of studying ECG signal filtering by analyzing the variance resulting from the exchange of positions of the filters of the cascading filter by ANOVA. Both methods yielded impressive results compared to previous recent work. Thus, we concluded that these two methods gave equivalent results, regardless of the method used. We have also provided an extension of the contribution to FPGA embedding by harnessing the Matlab Simulink SG, connected to the XILINX ZedBoard, the magnificence of this contribution having received remarkable results of great interest in the field of embedded systems.

Keywords: ECG, Cascade, FIR, Noise, SNR, MSE, Window, PTB database, Disparity, Diagnostic.

Résumé

Cette thèse contient une étude complète du signal de l'électrocardiogramme, car elle comprend plusieurs chapitres interdépendants contenant une série d'informations sur le cœur humain. L'étude s'est concentrée sur l'élimination du bruit à l'aide d'une méthode de filtrage séquentiel de trois filtres FIR. Dans le premier article, la méthode consiste à étudier la purification du signal d'électrocardiogramme par sélection de fenêtres combinées à des portions de filtre successives. Le deuxième article, contient la méthode d'étude du filtrage du signal ECG en analysant la variance résultant de l'échange de positions des filtres qui composent le filtre en cascade par ANOVA. Les deux méthodes ont donné des résultats impressionnants par rapport aux travaux récents précédents. Ainsi, nous avons conclu que ces deux méthodes donnaient des résultats équivalents, quelle que soit la méthode utilisée. Nous avons également fourni une extension de la contribution à l'embarquement FPGA en exploitant le Matlab Simulink SG, connecté au XILINX ZedBoard, la magnificence de cette contribution ayant reçu des résultats remarquables d'un grand intérêt dans le domaine des systèmes embarqués.

Mots clés : ECG, Cascade, FIR, Bruit, SNR, MSE, Fenêtre, Base de données PTB, Disparité, Diagnostic.

Introduction

Cardiovascular disease is the most common cause of death worldwide, heart rhythm disorders and related pathologies are rising. They result in a heart that beats too slowly, too fast or in a disorderly manner; and often require specific equipment (pacemakers, defibrillators).

Therefore, the diagnosis of these diseases is a vital task. To perform this procedure, several tools are used, including the electrocardiogram (ECG).

The ECG is the oldest and most widely available physiological test. It helps to identify cardiovascular diseases. However, in a real scenario, the quality of the signals measured by this type of device can be degraded by different sources of interference. The signal is affected by several different types of noise, such as electromyography (EMG) noise, high-frequency noise (additive Gaussian white noise and power line interference (PLI), and low-frequency noise (wandering of the baseline), during its acquisition and transmission.

The signal's nonlinear and non-stationary nature and the noises that affect it constitute an obstacle. The need to overcome these obstacles is the cause of various approaches and techniques for its treatment; one of the approaches used for ECG signal processing is filtering.

ECG signals are generally in analogue form; these signals transform a processing chain (amplification, sampled and quantified) to pass from the continuous domain, output from a sensor, to the discrete domain, interpretable by a machine [1]. Signal operations in the discrete domain are much more efficient with the rapid improvement in information technology. The most common method of recovering the desired information from a signal is filtering. The filters are in the continuous domain, with analogue signals, or in the discrete domain, with digital signals.

FIR (Finite Impulse Response) filters are typically chosen for applications where the linear phase is essential, and a decent amount of memory and computational performance is available. They are widely used in biomedical signal enhancement applications. Their all-zero structure (discussed below) ensures they never become unstable for any input signal, giving them a distinct advantage over IIR filters.

Multiple algorithms for filtering a signal have advantages and disadvantages in the temporal, frequency and phase planes. Several filtering approaches dedicated to the ECG signal have

been studied in the literature. Some of them use classical filtering approaches such as analysis by discrete wavelet transforms (DWT) [2-3], the principle of smoothing by the use of the Savitzky-Golay filter for the step of preprocessing [4], adaptive filtering in [5, 6] and digital filter in [7]. Others use advanced methods based on artificial intelligence and deep learning [8] or deep factor analysis to eliminate a noise signal with Gaussian distribution proposed by Ge Wang et al. [9].

The filter is made analogically by electronic circuits consisting mainly of passive elements (resistors, capacitors, and inductors) and active elements (transistors or integrated circuits operational amplifiers) or digital circuits using lap computers, a CPU and memory. Digital filters are, in most cases, a part that integrates a real-time on board device.

The notion of real-time embedded operation leads us to introduce progress on the integration capabilities of electronic circuits, which have opened up new perspectives for real-time signal processing on embedded systems. On the one hand, specific processors can commonly perform billions of operations per second, and on the other hand, reprogrammable components comprise several billion logic gates. These circuits make it possible to carry out applications with performance in terms of constantly increasing processing speed. [10].

In this context, the Field Programmable Gate Array (FPGA), with its great integration and reconfiguration capabilities, make it a critical component for rapidly developing prototypes through the use of development environments such as Quattus from Intel-Alter and Vivado from Xilinx intended even for non-experts.

This thesis aims to study ECG signal noise removal methodologies based on FPGA application. The thesis is organized as follows:

First, it provided several pattern recognition, human heart function and anatomy methodologies, ECG databases, and resources.

• In Chapter 2, discusses ECG signal filtering techniques emphasizing improving the generalization ability.

• Chapter 3 includes SoC for the embedded system. In this chapter, we give particular importance to programmable circuits.

• Chapter 4 covers the purpose of this thesis, where we adopt the windows selection algorithm, modifying the optimization criterion to select a digital filter design with greater generalization.

This chapter comprehensively explains the published articles [11] and [12] results and then the results of the extension of the embedded system using an FPGA application based on the XILINX DIGILENT board.

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Chapter I: Anatomy and functionality of the human heart

1.1Introduction

Before looking into the details of advanced ECG processing and FPGA implementation, it is essential to understand the physiology of the heart and how to measure the electrical activity of the heart's conduction system. This is important because the following chapters address noise suppression issues in ECG signals and propose new algorithms to reduce ECG signal distortion. Therefore, a brief introduction to cardiac physiology and anatomy is included in this chapter.

The different patterns in which experts analyze the electrical activity of the heart's conduction system are presented. Monitoring devices such as Holter Monitor are introduced to understand the traditional path with new technology applied to the recorded signal before it reaches the hands of experts. The PTB diagnostic electrocardiogram database is presented with some details, which in turn have achieved the announced contributions in the last chapter of this thesis. Finally, most challenges and problems while obtaining an ECG signal are presented and discussed.

1.2Cardiovascular system

The heart is a muscular organ pump that pumps oxygenated blood to the whole body through the circulatory system. The heart is located in the medial thoracic cavity to the lungs and posterior to the sternum. The heart has four chambers: the right and left atria and the right and left ventricles. Several AV and AV nodes are also seen in the heart. Appearance. Figure 1.1 represents the blood flow diagram of the human heart. The left and right ventricles are located in the heart's lower chamber, while the right and left atria are located in the upper chamber of the heart. The atria are connected to the ventricles by fibrous, non-conductive tissue that keeps the atria electrically isolated from the ventricles.

The circulation of blood through the heart is divided into two phases: systole and diastole. Systole is the period of contraction of the ventricular myocardium, while diastole is the period of dilation of the ventricular cavities of the heart [1]. It receives impure and deoxygenated blood through the veins and pumps it to the lungs for purification. Deoxygenated blood is obtained through large veins such as the superior and inferior vena cava and flows into the

right atrium. The right atrium contracts and pushes blood into the right ventricle. At this time, the ventricle is tightened, and the pumping efficiency, i.e. contraction, is maximized. The blood then travels from the right ventricle to the lungs for purification. The left atrium receives purified blood from the lungs. During atrial systole, the purified blood in the left atrium goes into the left ventricle through the mitral or bicuspid valve. The left ventricle contracts and pumps pure blood to the rest of the body through the aortic valve and aorta [2], [3]. During the ventricular diastolic period, oxygenated blood reaches the left ventricle from the left atrium by opening the mitral valve, and deoxygenated blood reaches the right ventricle from the right atrium by opening the tricuspid valve. In the systolic period of the heart ventricle, the oxygenated blood is pumped out from the left ventricle to the body by opening the aortic valve through the aorta, and the deoxygenated blood goes to the lungs from the right ventricle by opening the semi lunar valve through the pulmonary artery. The heart's function is to regularly contract and pump blood to the lungs for oxygen and then pump this oxygenated blood for general circulation. This perfect rhythm is continuously maintained by the electrical signals generated by the pacemaker.

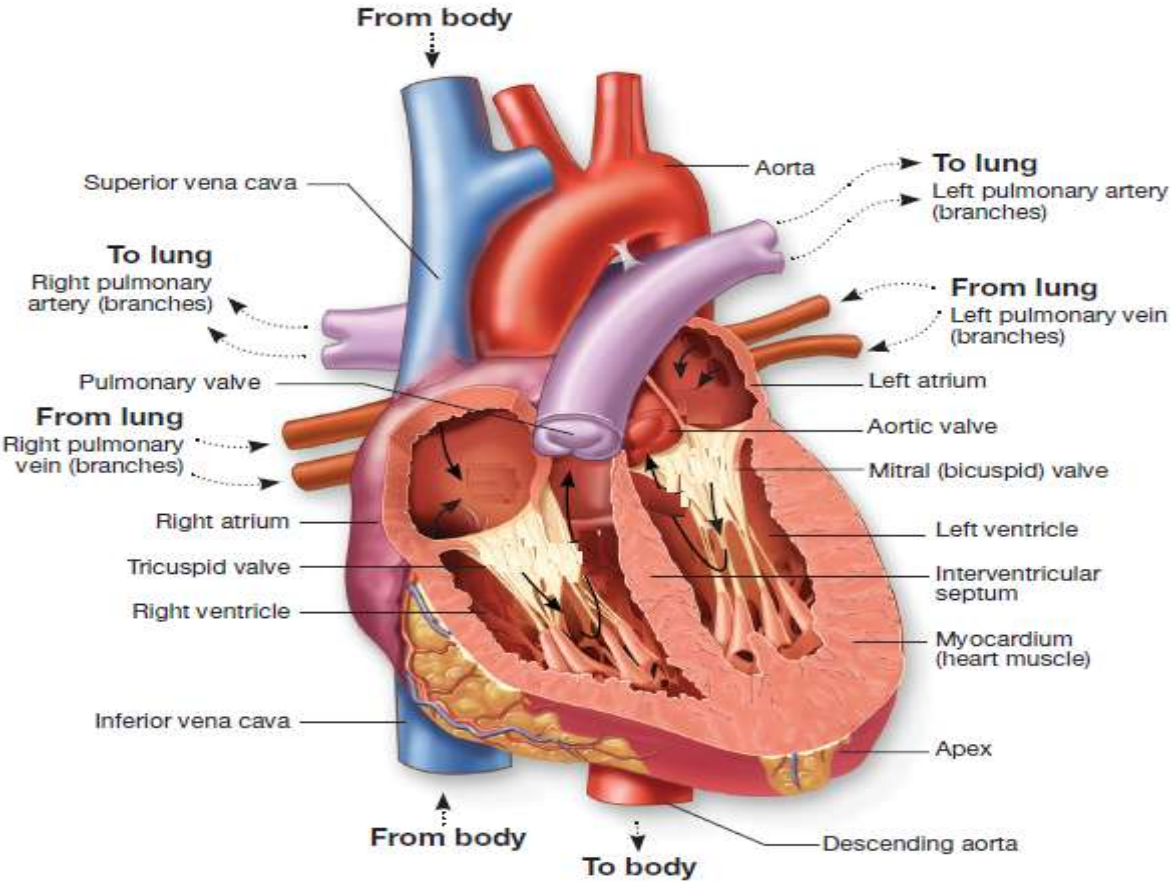

Figure 1.1: movements of the walls and valves (arrows)

Made up of the heart and vessels (arteries and veins), the function of the cardiovascular system is to distribute to organs through the blood oxygen and nutrients essential to their life while eliminating waste.

1.2.1 Arterial and venous circulation

The blood circulates within a network made up of "pipes" in figure 1.1, with calibres perfectly suited to their functions

1. Arteries, from the large aorta (2.5 centimetres in diameter) to small arterioles (no more than 2 millimetres), carry oxygen-laden blood from the heart to the organs.
2. The thin "like hair" capillaries ensure blood circulation inside each organ.
3. The veins bring the carbon dioxide-laden blood back to the heart.

1.2.2 The heart of the human body

The heart, enveloped in the pericardium, is located in the anterior mediastinum between the two lungs, on the left diaphragmatic dome, behind the sternum and the anterior costal grill and in front of the posterior mediastinum, especially the oesophagus.
Responsible for blood circulation, the heart is a muscle, reddish-brown, which weighs about 250 g in adults: It has the shape of a triangular pyramid with the top at the bottom, to the left and in front; the base looks up, back and right; its central axis is oblique down, forward and to the left.
The three faces are anterior, inferior and left lateral.
Two deep furrows cross them:

1. The atrioventricular groove, in the plane perpendicular to the major axis of the heart, separates the atrial mass behind from the more anteroinferior ventricles,

2. The inter-ventricular groove, then the inter-auricular groove perpendicular to the previous one. It corresponds to the plane of separation between the right heart and the left heart.
The furrows contain fat and the main branches of the coronary vessels.

The heart (Figure 1.1) is a hollow organ made up of the right heart and left heart, completely separate. The atria are separated by a septum called the inter- atrial septum and the ventricles by the inter-ventricular septum.

1.2.3 Cardiovascular physiology

The heart can be considered as a double muscular pump (right heart and left heart):

1. Essentially driven by the myocardium of the right and left ventricles,
2. Functioning thanks to the nodal tissue (where cardiac automatism is born) and to the coronary blood circulation (providing oxygen and energy and evacuating cloudy waste),
3. Pulsing the blood synchronously in the pulmonary and systemic circulations, which feedback on its functioning,
4. Adapt the blood flow it produces to the organism's needs thanks to a nervous and humoral regulatory system.

1.3 Functioning of the heart

1.3.1 The Cardiac mechanical activity

The heart propels blood through contractions of its muscle tissue called the myocardium. This cycle repeats itself constantly, and consists of three distinct phases see Figure1.2

- Atrial systole: The contraction of the atria and the ejection of blood to the ventricles, the closing of the atrioventricular valves and the presence of a severe noise of the heart (represents 1/6 of the cycle).

- Ventricular systole: a contraction of the ventricles and the ejection of blood to the organs.

- closure of sigmoid or arterial valves (aortic on the left and pulmonary on the right) and the presence of acute heart noise (represents 1/6 of the cycle).

- Diastole: relaxation of all parts of the heart, passive filling (represents 2/3 of the cycle).

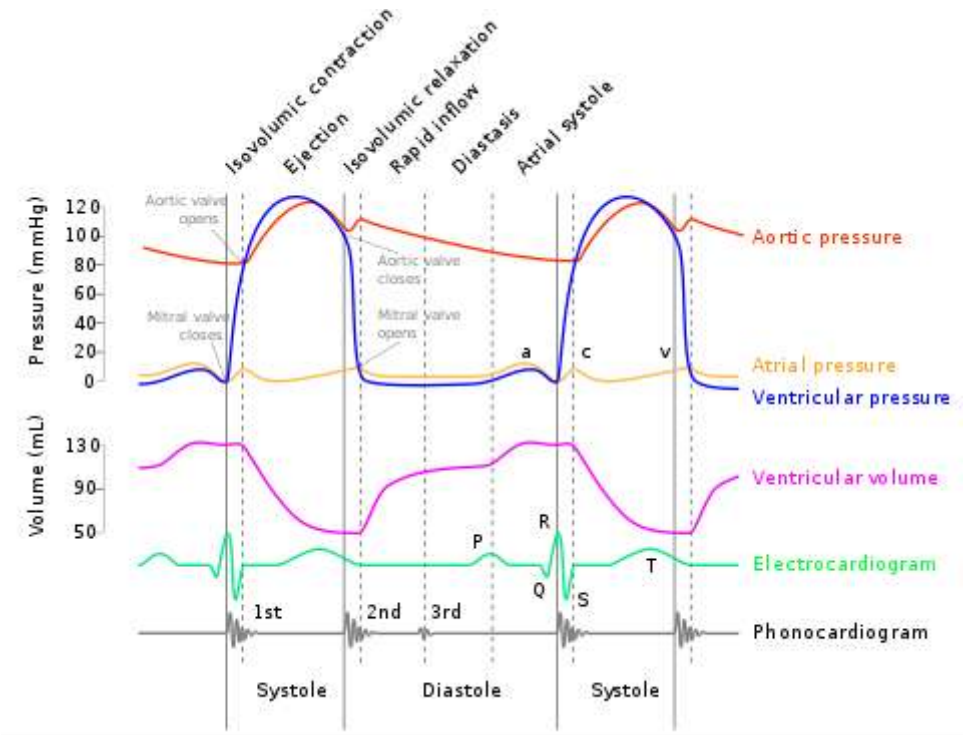

Figure 1.2 Wiggers diagram of the cardiac cycle.

Events of the cardiac cycle for left ventricular function, displaying adjustments in left atrial pressure, left ventricular pressure, aortic pressure, ventricular volume, and the electrocardiogram.

1.3.2 Electrical activation of the heart

1.3.2.1 Potential for rest and action

At rest, myocardial cells are "polarized" with a predominance of positive charges on the outside and negative charges on the inside.

If two microelectrodes connected to a galvanometer are placed one extracellularly and the other in a cell, a stable potential difference is registered, different according to the cell type, of the order of - 90 mV for a ventricular cell: it is the transmembrane resting potential (Vr).

If the cardiac fibre is stimulated, an action potential in figure 1.3 appears, which reflects the variations in the transmembrane Potential as a function of time.

These variations result from ionic movements across cell membranes.

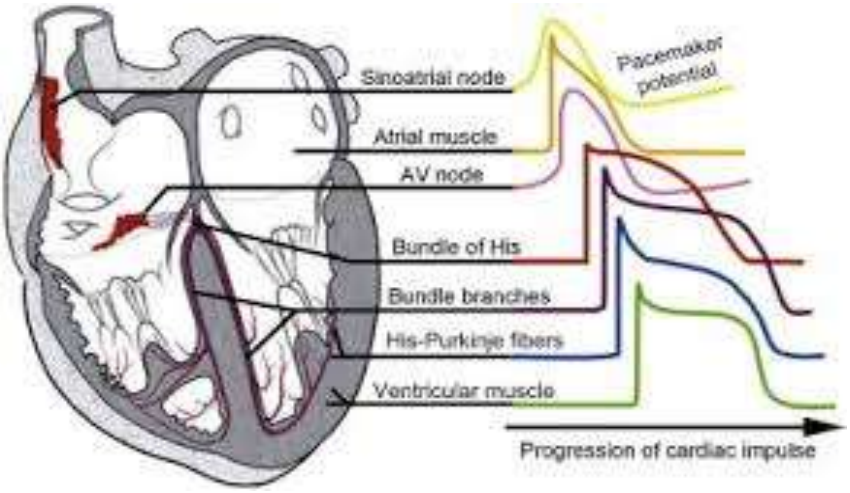

Figure 1.3 The Potentials of the nodal tissue.

In widespread heart, cells may be grouped into sorts: those from the SCS and the contractile cells. The first is accountable for the era of the electric impulse (rhythm city) and its conduction to the contractile cells, at the same time as the contractile cells are answerable for the pumping or mechanical function. Both cellular sorts are liable for the electromechanical link. Figure 1.4 for its miles proven the waveforms of the voltage or motion potential, and currents measured inside the cell membrane of a contractile cellular. Following the depolarization stages inside the equal Figure, observe that Na channels are activated after a cellular gets depolarizing cutting-edge, ensuing in an internet inward advanced manifested as segment zero of the AP.

Phase one begins with the outlet of speedy outward potassium cutting-edge.

Phase two or the AP's plateau segment results from an L-kind Ca cutting-edge that counteracts the outward K currents. With time, L-kind Ca channels are inactivated, and the plateau subsides. At the same time, the boom in calcium awareness acts as a cause for the discharge of greater Ca saved within the sarcoplasmic reticulum, which in flip offers contraction signs to the myocyte contractile elements, generating the contraction of the cellular.

Phase three is because of "behind schedule rectifier" outward K currents.

Phase four constitutes a steady, stable, polarized membrane because of voltage-regulated inward rectifiers. Compared to an atrial motion potential, ventricular AP has an extended duration, a better segment 2, a shorter segment three, and a more significant bad segment four.

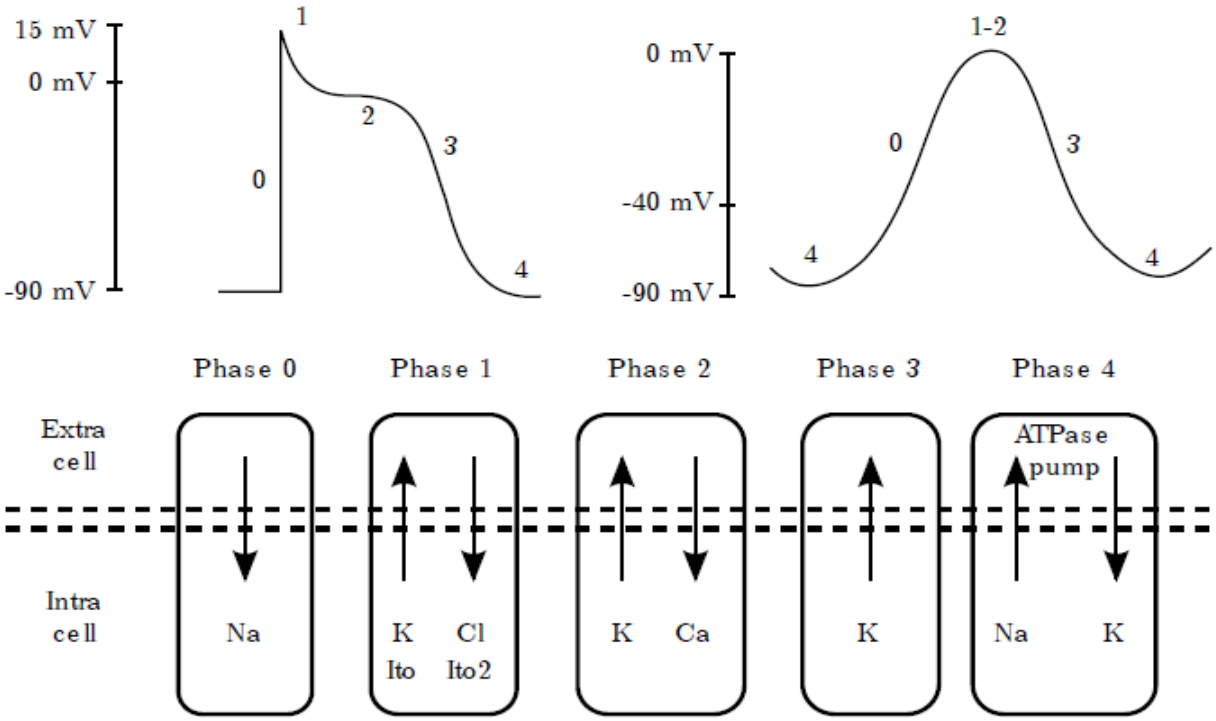

Figure 1.4 The action potential in the cells

Top panel: on the left, the motion capacity in contractile cells, and the proper in SCS cell. Bottom panel: most important currents for the duration of the exceptional stages of Na-channel-based motion capacity [4].

Alternatively, the SCS cells can generate a spontaneous motion capacity by using T-kind Ca and K rectifier currents. These currents confer the volatile electric belongings of section 4, inflicting those cells to increase rhythmic spontaneous sluggish diastolic depolarization. Furthermore, once AP reaches –forty mV, L-kind Ca channels are activated, producing the slow upstroke of the motion capacity in those styles of cells (section 0).

There are 3 styles of SCS cells:

1. P cells, discovered primarily with inside the sinus node, are answerable for automaticity.
2. The Purkinje cells are discovered with inside the His package branches and are answerable for the short transmission of electrical impulses via the ventricles.
3. The transitional cells, with sluggish conduction velocity, are generally discovered among the P, Purkinje and contractile cells.2.1.5.2

1.3.2.2 Automation

Cardiac automatism is the production by the nodal tissue of repetitive electrical activity, with each electrical impulse (action potential) causing the heart to contract. This electrical activity is produced by spontaneous ionic exchanges (slow diastolic depolarization) across the membrane of nodal tissue cells to reach the threshold potential that triggers the action potential. Then occurs a complete restoration (repolarization).

Physiologically, the cells of the sinus node in Figure 1.5 control the heartbeat, which is called sinus rhythm. The frequency of this rhythm is constantly modulated according to the body's needs by neuro -humoral regulation. (Acceleration under the effect of the sympathetic and catecholamines, slowing down under the impact of the parasympathetic).

In pathology, the origin of the automatism may not be sinus: either when an abnormal tachycardia occurs whose natural frequency exceeds that of the sinus node which is thereby inhibited, or when the sinus node is deficient, another cell group tissue then takes over to generate cardiac automatism.

1.3.2.3 Heart Conduction

The action potentials generated by the nodal tissue are conducted at high speed to the cells of the common myocardium.

Physiologically, the nascent rhythm in the sinus node Figure 1.5 activates the atrial myocardium and reaches the atrioventricular node and the trunk of His bundle. This activity then reaches the right and left branches of the bundle of His, the Purkinje cells and finally the cells of the ventricular myocardium.

The interventricular septum is depolarized from left to right, then the ventricles from the endocardium to the epicardium. This "nodo-hissian" pathway is the only possible electrical passageway from the atria to the ventricle through the fibrous skeleton of the heart.

In pathology: conduction can be deficient at all levels leading to the risk of transient (syncope) or permanent (sudden death) arrest of cardiac activity.

Conversely, there may be additional conduction pathways between the atria and the ventricles called pre-excitation pathways that can expose patients with severe heart rhythm disturbances.

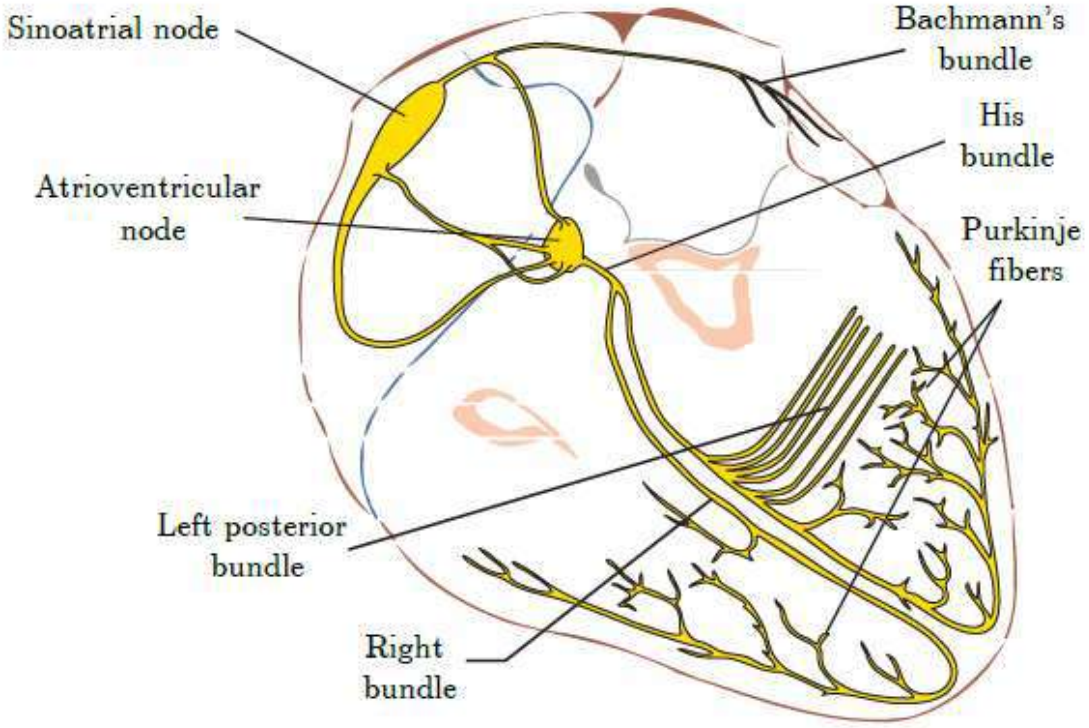

Figure 1.5 electrical conduction system of the heart

1.3.2.4 Excitation and contraction coupling

At their level, the electrical excitation of the cells of the common myocardium by the nodal tissue causes significant ionic movements (especially calcium), triggering the shortening of contractile proteins (actin and myosin). As a result, all myocardial cells receive an electrical pulse briefly (6-8 / 100 seconds) to contract in a coordinated fashion and generate cardiac blood ejection.

This coupling is responsible for an electromechanical delay explaining that the ventricular diastole (see below) is contemporaneous with the "QRS" ECG complex of depolarization (see ECG), and the mechanical systole (see below) of the T wave (see ECG).

1.3.2.5 Coronary circulation

The coronary blood circulation must ensure myocardial perfusion is adapted instantly to the heart's needs.

It is subject to specific constraints:

1. The heart is never at rest,
2. The myocardial oxygen extraction from the coronary arterial blood is almost maximal upon rest (greater than 60%).

As a result, the increase in the myocardial oxygen supply (during exercise), is done essentially by increasing the coronary blood flow and not the oxygen extraction; the ventricular systolic contraction "crushes" the coronary circulation, which rests.

1.3.2.6 Coronary blood flow

This is the amount of blood delivered to the myocardium per minute. Its increase during exercise, thanks to complex regulation, is significant since it can be multiplied by 3 or 4 compared to rest (concept of coronary reserve). This increase ensures increased myocardial metabolic requirements (oxygen and substrates) during exercise. The regulation of coronary blood flow depends on many hemodynamic and neuro-humoral parameters, including endothelial secretions (N0 in particular).

1.3.2.7 Myocardial metabolism

It is primarily aerobic (consumes oxygen). In clinical practice, this myocardial oxygen consumption (MVO2) can be assessed by the product heart rate (F) multiplied by systolic arterial pressure (PAS) because the variations of this MVO2 are well correlated with those of this product.

The substrates used are mainly fatty acids (65%), glucose (20%), and lactates (15%). It is strongly oriented towards the production of energy necessary for the activity of the heart's contractile proteins.

1.3.2.8 Myocardial ischemia and necrosis

Insufficient blood supply to a myocardial area compared to requirements causes ischemia, which generates symptoms (see angina) or complications.

If this ischemia is profound and / or tasting, the myocardial cells will be destroyed in the affected area. This is myocardial ischemic necrosis.

1.4 Cardiac cycle

The above-described routine electrical activity generates mechanical activity of the heart, dominated by contraction and then relaxation of the ventricles (contraction of the atria has only a limited impact on normal heart function). The succession of ventricular systole and ventricular diastole forms a cardiac cycle.

1.4.1 Ventricular systole

The contraction of the two ventricles is synchronous and lasts about a third of a second at rest. Its onset coincides with the closure of the atrioventricular valves, followed by the opening of the aortic valve and pulmonary sigmoid.

During systole, intraventricular pressures (Figure 1.6) increase sharply, allowing blood to be ejected from the right ventricle to the pulmonary artery and blood from the left ventricle to the aorta.

With the atrioventricular valves closed, there is no backflow to the atria.

The quality of systolic blood ejection depends on:

1. The contractility of the ventricular myocardium, an intrinsic property of myocardial cells which deteriorates in heart disease,
2. The ventricular preload,
3. Ventricular after load.

The ventricular contraction decreases rapidly at the end of systole, and then diastole appears.

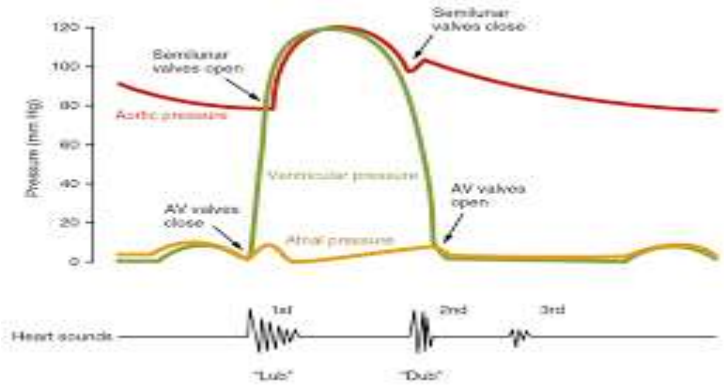

Figure 1.6 different times and evolution of intracavitary pressures

The pressure curves of the left atrium, ventricle, and aorta are superimposed (for the right heart, the diagram is identical except for the pressure levels).

Abbreviations: Ao: aorta; OG: left atrium; LV: left ventricle.

Between the closing of the mitral valve and opening of the aortic valve = Isovolumic Contraction phase.

4. Between opening and closing of the aortic valve: Ejection phase.

5. Between the closing of the aortic valve and opening of the mitral valve: Isovolumic Relaxation phase.

6. Between the mitral opening and closing: ventricular filling.

7. Between B1 and B2 are the isovolumic contraction and ejection phases.

1.5 Electrocardiogram ECG

The ECG signal represents the heart's electrical activity and is arguably the most widely used diagnostic technique for cardiac pathologies. The ECG is a non-stationary random signal structured by the succession of waveforms and intervals (P, Q, R, S, and T).

Any morphological or temporal modification of its events (or chronic) constitutes a cardiac pathology. For example, changes in rhythm or frequency are cardiac arrhythmias (fatal diseases) and are the subject of this work.

The history of the ECG is around the 1880s when Augustus Waller and E Marey De Silva [5, 6] showed the possibility of skin-based monitoring of the heart's electrical activity. British physiologists John Burden Sanderson and Frederick Page recorded this activity with the capillary electrometer a few years earlier [7]. They were shown to be composed of two phases (later called QRS and T). In 1887 Augustus D. Waller published the first human electrocardiogram, while in 1895; Willem Einthoven defined the five deflections P, Q, R, S and T [8]. He used the string galvanometer in 1901 and published the first classifications of pathological electrocardiograms in 1906. In 1924 he won a Nobel Prize for his work on electrocardiography.

An electrocardiogram (ECG) is a graphical representation of the heart's electrical activity. This electrical activity is linked to variations in the electrical Potential of cells specialized in contraction (myocytes) and cells specialized in the automatism and conduction of impulses. Electrodes collect it on the surface of the skin.

1. The ECG is the paper trace of electrical activity in the heart.
2. The ECG machine is the device for doing an ECG machine.
3. The electro-cardio-scope, or scope, is a device that displays the waveform on a screen.

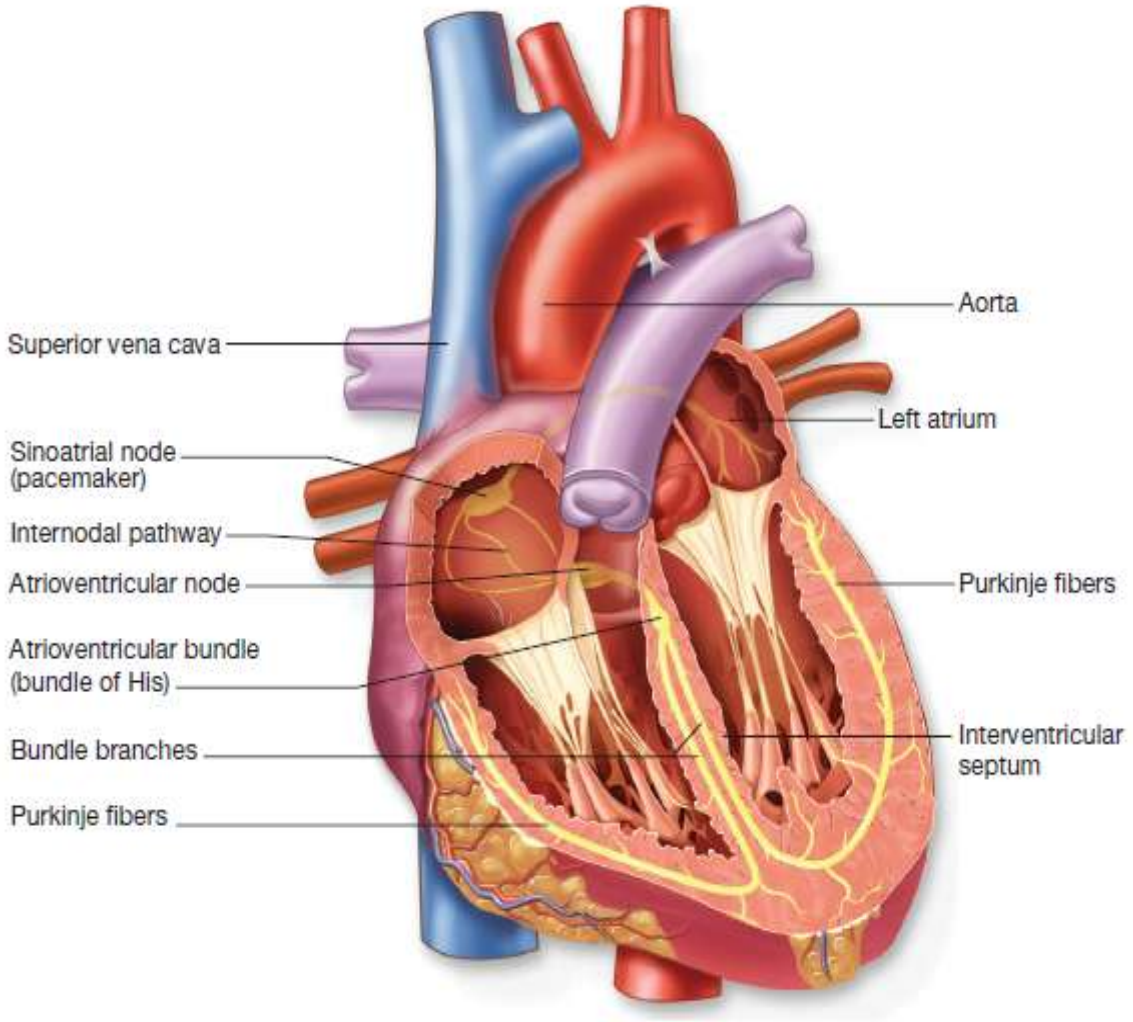

Figure 1.7 electrical system in the heart

The electrocardiogram, known as an ECG, is a dimension of the electric hobby of the heart (see Figure 1.8). This can provide the medical doctor statistics approximately the fitness of the heart, especially the myocardium.

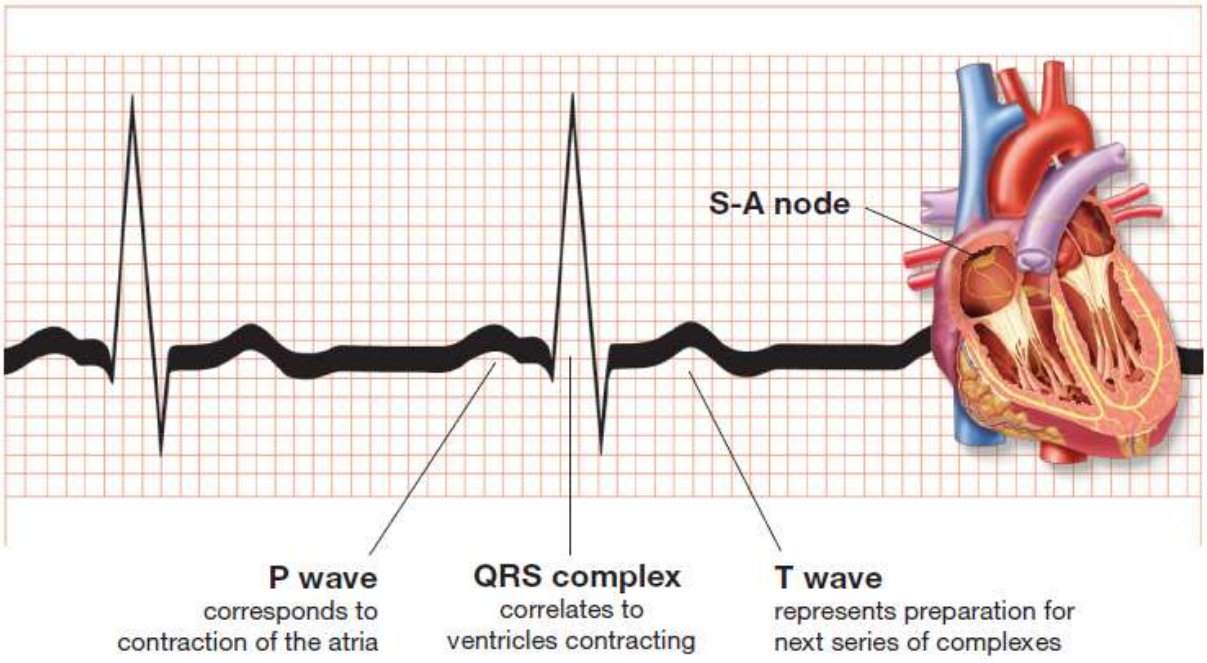

Figure 1.8 an electrocardiogram ECG wave's document of the electric sign because of its movements via the conduction machine of the coronary heart. This sign stimulates the chambers of the coronary heart to an agreement and loosens up with inside the right sequence.

1.5.1 ECG Waves and Intervals

The recorded trace, called an electrocardiogram (ECG), presents a characteristic appearance; its deformities are a sign of abnormalities in the functioning of the heart. Any interpretation of the ECG refers to the shape and wave width characteristics of the normal ECG signal shown in Figure 1.9.

P wave: It corresponds to the depolarization of the atria from the sinus node to the atrioventricular node. It can be positive or negative; with around 90 ms. This is the wave that precedes the QRS complex. Usually, it is difficult to see on the ECG, especially under noisy conditions.

QRS complex: It corresponds to the ventricular depolarization preceding the mechanical effect of contraction. It has the most significant amplitude of the ECG signal and is composed of three contiguous waves that follow the P wave; a wave called Q first of negative amplitude,

a wave called R positive in a normal ECG and finally, the 'S wave, which is negative. The normal duration of the QRS complex is between 85 and 95 ms.

T wave: It corresponds to the repolarization of the ventricles; it can be positive, negative or biphasic. This is the wave that follows the QRS complex after returning to the isoelectric line (except for specific pathology); its amplitude is lower than that of the QRS complex.

PR Interval: The PR interval, which has a duration between 0.14 to 0.2 seconds measured

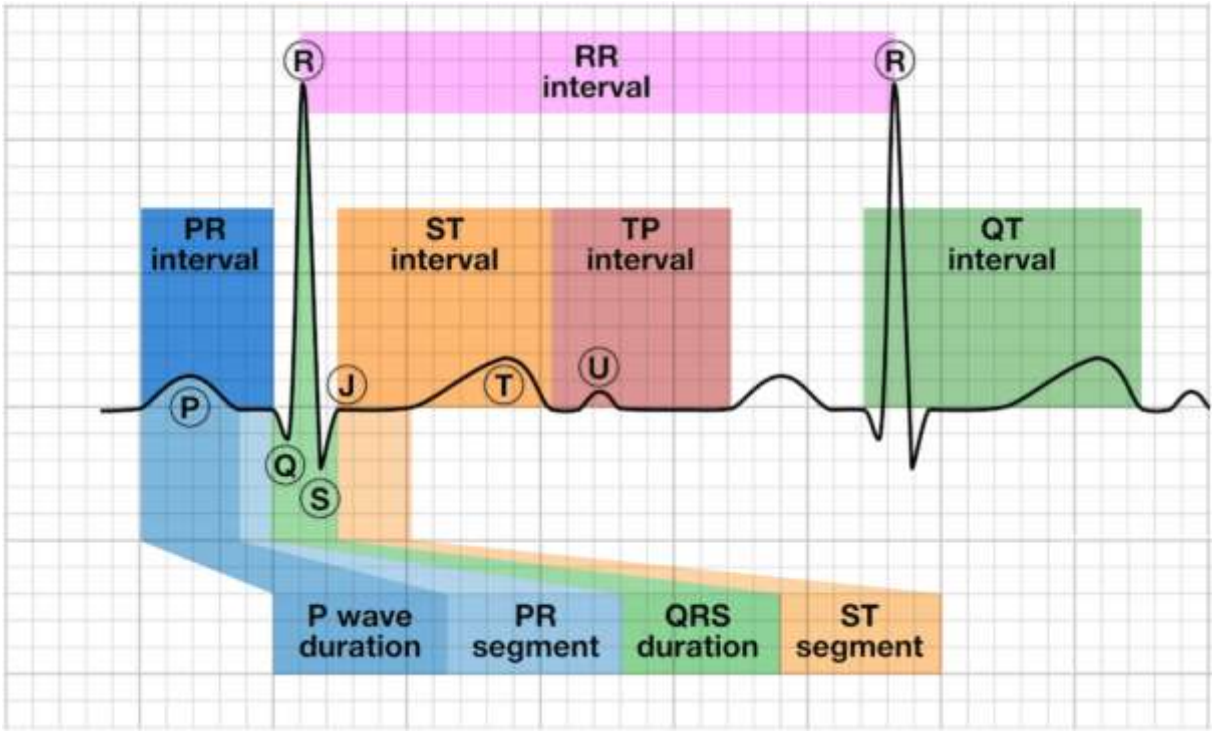

Figure 1.9 Electrocardiogram ECG trace

Between the onset of the P wave and the onset of the QRS complex, that is, the time between depolarization of the atria and the AV node. This time is required for an electrical impulse to pass from the sinus node to the ventricles, and it is used for detecting arrhythmia and heart rate variability.

ST-segment: Or the duration of complete stimulation of the ventricles. It is the interval during which the ventricles remain in an active depolarized state. This is the time between the end of the S wave and the start of the T wave.

PQ interval: This is the time interval between the onset of depolarization of the atria and that of the ventricle. This is the propagation time of the electrical impulse from the sinus node to the ventricles. It is measured between the onset of the P wave and the onset of the QRS complex.

QT interval: This interval corresponds to the time of ventricular systole, which goes from the start of excitation of the ventricles until the end of their relaxation. This is the time between the onset of the QRS complex and the end of the T wave.

1.5.2 Derivatives

The ECG signal records the heart's electrical activity by electrodes on the body's surface. Depending on their location, there are different derivations. The standard ECG is recorded on 12 leads (six limb leads and six precordial), with a paper speed of 25 mm per second and an amplitude of 10 mm at 1 mV. In what follows, we will represent the different standard leads of the clinical ECG and the ambulatory Holter recording, the terminology of waves and intervals used for the analysis of the ECG, and the different rhythm and cardiac conduction disorders. With details, the various artefacts visible on the ECG during recording.

1.5.2.1 Three bipolar leads (or standard leads)

Bipolar or so-called standard leads were proposed by Einthoven [9] at the start of the twentieth century and are still used today. They allow the study of the heart's electrical activity on the frontal plane. These three signals are the potential difference between distant points on the body.
We distinguish:

1. Lead I (DI): Bipolar measurement between left and right arm.

$$DI = VL - VR \tag{1.1}$$

2. Lead II (DII): Bipolar measurement between left leg and right arm.

$$DII = VF - VR \tag{1.2}$$

Lead III (DIII): Bipolar measurement between left leg and left arm.

$$DIII = VF - VL \tag{1.3}$$

Where VR corresponds to the Potential of the right arm, VL corresponds to the Potential of the left arm, and VF corresponds to the Potential of the left leg. The right leg is connected to the mass. The resulting vectors then form an equilateral triangle called the Einthoven triangle as shown in Figure 1.10.

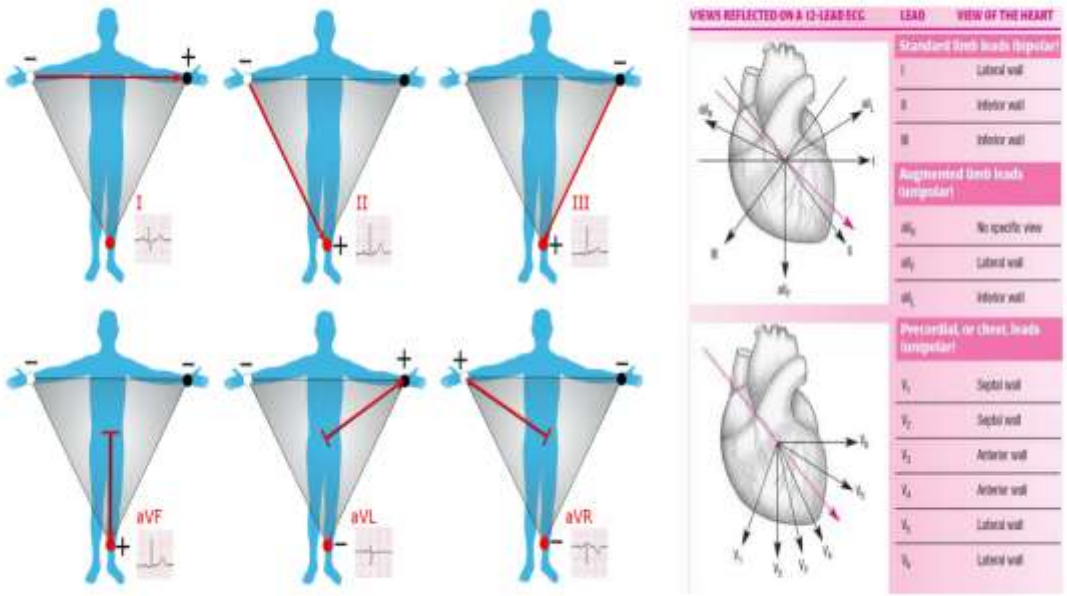

Figure 1.10 The derivations of Einthoven

1.5.2.2 Three unipolar leads

These leads also allow us to study the variation of electrical activity on the frontal plane. They were determined by Wilson [11] in 1934 and improved by Goldberger [12].

They allow us to obtain signals of greater amplitude. Each signal represents the difference between the Potential of one electrode and the average of the potentials collected by the other two electrodes. These derivations are known as aVR, aVL and aVF; where "a": augmented

voltage; that is to say, each potential collected is amplified. The "V" means this is a unipolar lead. "R", "L" and "F" is (Right, Left, Foot).

These leads are shown in Figure 1.10 bottom, and the voltages are calculated as follows:

$$aVR = VR - \frac{VL+VF}{2} \quad (1.4)$$

$$aVL = VL - \frac{VR+VF}{2} \quad (1.5)$$

$$aVF = VF - \frac{VL+VR}{2} \quad (1.6)$$

Six precordial derivations are unipolar derivations proposed by Wilson [13]. The exploration electrodes are placed near the heart at specific points on the thorax. They allow us to obtain the leads V1 to V6. Each Potential is calculated concerning the average value of the potentials VR, VL and VF. These leads will enableus to measure the heart's electrical activity horizontally. Figure 1.11 shows the location of the electrodes on the chest.

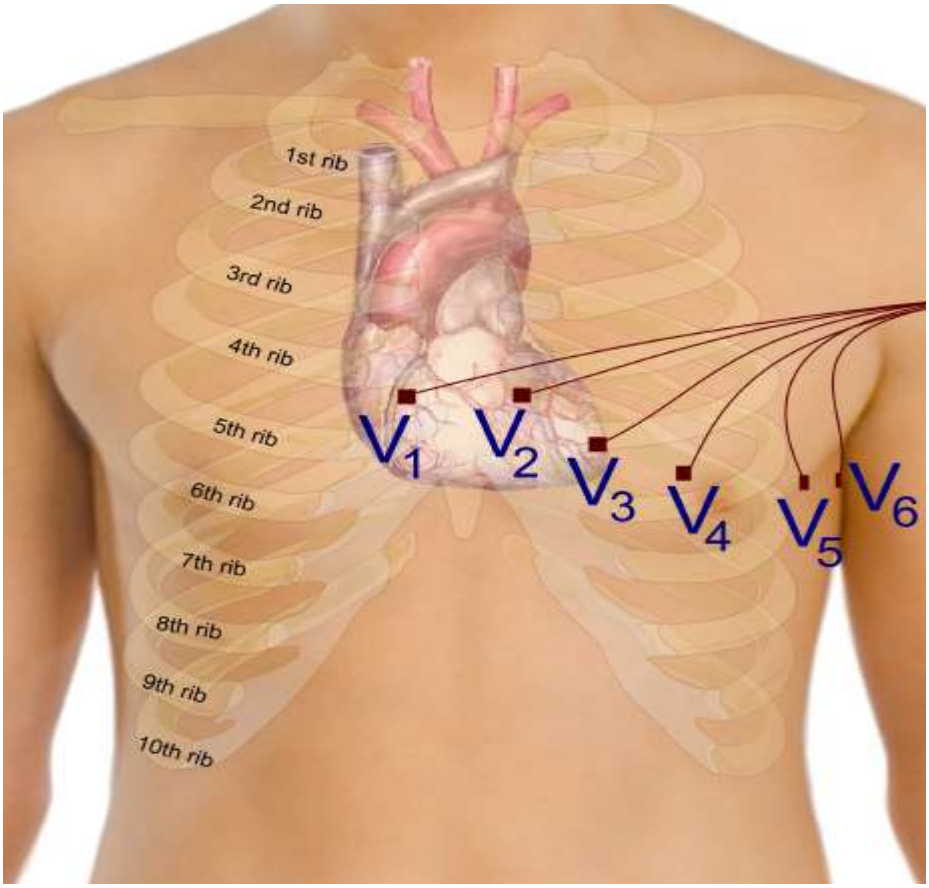

Figure 1.11 Unipolar precordial leads

1.6 ECG Monitoring Devices

Several devices are used for ECG monitoring systems. These devices are typically mobile, wearable, and sensor-based. These ECG monitoring devices are smartphones, smartwatches, and handheld ECG monitors. Aljuaid et al. [14] assessed the importance and effectiveness of smartphone-based ECG monitoring devices on the frequency of clinic visits of patients who had AF ablation. This study proved that usingthe "ECG monitoring" application on smartphones leads to a large and significant reduction in inpatient visits to the clinic after surgery. Similarly, a few mobile monitoring devices integrate an Arduino microcontroller with various sensors, including an ECG sensor, these devices have been used to retrieve sensory data and display vital sign measurements and then alert with notification messages the location of the user to the health care provider if an abnormality is discovered [15]. A combination of microcontrollers such as Arduino with system-based smartphones has been developed to realize an intelligent healthcare system dedicated to elderly patients for home medical services [16]. The system incorporates an artificial bee colony (ABC) algorithm for detecting the R ECG peak. This system also detects various abnormalities (arterial hypertension, arterial hypotension, fever, tachycardia and bradycardia) and sends notifications in case of unexpected events.

1.6.1 Traditional ECG Monitoring

Other research has touched on traditional ECG monitoring setups in hospitals [17,18,19], homes, or remote ambulatory settings [15,16]. Screening devices can be linked to treatment devices or accessed wirelessly [20,]. In many research studies, immobile ad hoc (i.e., one-time) monitoring has been deployed to address various healthcare situations using different ECG sensors and monitoring types. The work of de Benini[20] designs a single-wire sensor for home remote monitoring; Yousef and Hau [15] use, in their mobile system (myVitalGear), an analogue heart rate sensor for general health monitoring. Rafik et al. [22] designed a device with three-lead wet electrodes for home health monitoring. Several researchers highlighted that ad hoc and non-mobile monitoring could reduce the burden of outpatient clinic visits and AF-related visits in the post-ablation period. In their study, Aljuaid et al. [21] show that traditional ad hoc home monitoring on smartphones can reduce the number of post-ablation patient visits by more than 50%. However, in ad hoc monitoring settings, patients may forget to perform monitoring tasks. In addition, it is vital for patients in critical health situations to have regular recurrent screenings. To solve this problem, some research work, episodic

monitoring is proposed by performing pre-programming at intervals. For example, in the work of Hsieh and Len [16], an alarm function in the system to remind the patient to use the screening device is integrated. This approach saves medical resources and allows the elderly to take care of themselves, thereby promoting their health. Continuous monitoring is necessary for critical and life-threatening cases in traditional settings, especially in intensive care units. Many research studies have focused primarily on neonatal patients, for example, Bambang et al. [17] and Bouwstra et al. [18], who designed intelligent vest-based continuous monitoring systems for babies born prematurely in the neonatal ICU (NICU). Alternatively, for older adults who move, Ahmed et al. [23] used IoT-based technology for wireless sensor nodes positioned in intensive care and nursing wards to provide continuous ECG monitoring of patients with severe cases and then transmit the signal to distant doctors.

Accuracy in these situations is vital; therefore, a significant challenge encountered in continuous and intelligent critical care monitoring is the need to select an appropriate filtering technique; since ECG signals are noisy, which need a suitable amplifying approach should be used, given that the ECG signal is measured in millivolts.

1.6.2 Real-Time ECG Monitoring

In some cases, cardiologists may recommend 24-hour Holter monitoring for patient monitoring. A Holter monitor is a 12-lead medical device that records the heartbeat and checks for unusual signs. It is usually uncomfortable to apply the Holter 12-lead device to the patient's body for 24 hours. Some attempts have improved the 24-hour Holter monitoring and utilized an adhesive patch that can be attached to the patient's body, reducing the number of required leads in a typical Holter. For instance, Karaoğuz et al. [24] used a BeyondCare device applied to the upper left upper region of the subject's chest beside the 12-lead Holter device simultaneously for palpitation assessment.Recent advancements in wireless ECG monitoring systems have produced a wide variety of real-time monitoring systems, ranging from wearable textile-based monitoring systems, such as intelligent shirts [25] and textile electrodes, to contactless [26] ECG monitoring systems. In real-time setups, patients can measure ECG signals while doing normal real-life activities [27]. This has allowed for more prompt assessment and medical intervention when necessary.

Furthermore, it substantially reduced the cost of healthcare expenses by lowering the number of hospital visits for traditional regular monitoring. For instance, Lee and Chung [25] designed an intelligent shirt that continuously measures ECG and acceleration signals

remotely in a real-time setup for health monitoring. Bianchi et al. [28] proposed using T-shirts and bed sheets with sensor electrodes to measure ECG signals and other vital signs to assess sleep and respiratory problems in real-life settings. Bsoul et al. [29] designed Med Assist, a continuous, real-time, single-lead, wireless monitoring system to diagnoses leep apnea. On the other hand, the authors of [30,31] designed washable long-term wearable sensors for fitness and activity monitoring. Despite the advantages of continuous monitoring in real-time setups, it generates an abundant amount of ECG signal data, giving substantial signal noise and artefacts caused by abnormal physical activities. This problem has been highlighted by many researchers [25, 28]. This, in turn, emphasizes the need for noise filters and smart feature selection algorithms. Alternatively, episodic monitoring was adopted in several kinds of research to limit the causes of motion artefacts and constrain the amount of generated ECG signal data, allowing for easier processing and analysis. For example, Yoon and Gho [26] utilized a commercial contactless ECG monitoring device for remote home telemedicine. Their experiments considered pre-programmed and pre-planned 3-time intervals focusing on the patient's resting state and post-exercise state. Lee et al [32]. investigated a mobile cardiopulmonary rehabilitation system with a wireless Holter ECG to give real-time feedback during exercise in home settings.Unlike the pre-programmed continuous monitoring approach, some researchers have preferred to adopt signal sampling techniques for event-based ECG monitoring.

Signal sampling algorithms convert continuous-time signals into discrete. Consequently, a considerable reduction is achieved in the number of processed signals and power consumption.

1.6.2.1 HOLTER monitoring

Holters are small electronics devices with electrodes, generally bylead wires [33]. Usually, they record 24 hours of ECG signals; however, some holders can register up to 7 days.
While wearing a holter, patients typically record their symptoms and function withtheir daily activities (see Figure 2.12). Activities that cause the electrodes to become loose orduring recording are exceptions. For instance, patients are asked to avoid taking a shower, swimming, or any activity causing an excessive amount of sweating. Once themonitor is returned, the data are analyzed in digital format using special analysis software.
Diaries are used to understand the correlation between analysis results on the one hand andactivities and symptoms on the other hand.

Physicians decide to go for this recording to observe occasional cardiac arrhythmias that are difficult to identify in a shorter period because their symptoms areinfrequent. In this case, the short duration of monitoring can be inadequate.

Analyzing software is crucial when dealing with holter signals due to the long duration ofthe recorded signal. On average, more than 100.000 beats should be delineated andanalyzed. Moreover, the presence of noises and artefacts in the HOLTER ECG signal isinevitable. Therefore, examining or browsing through such a long signal would be highly time-consuming.

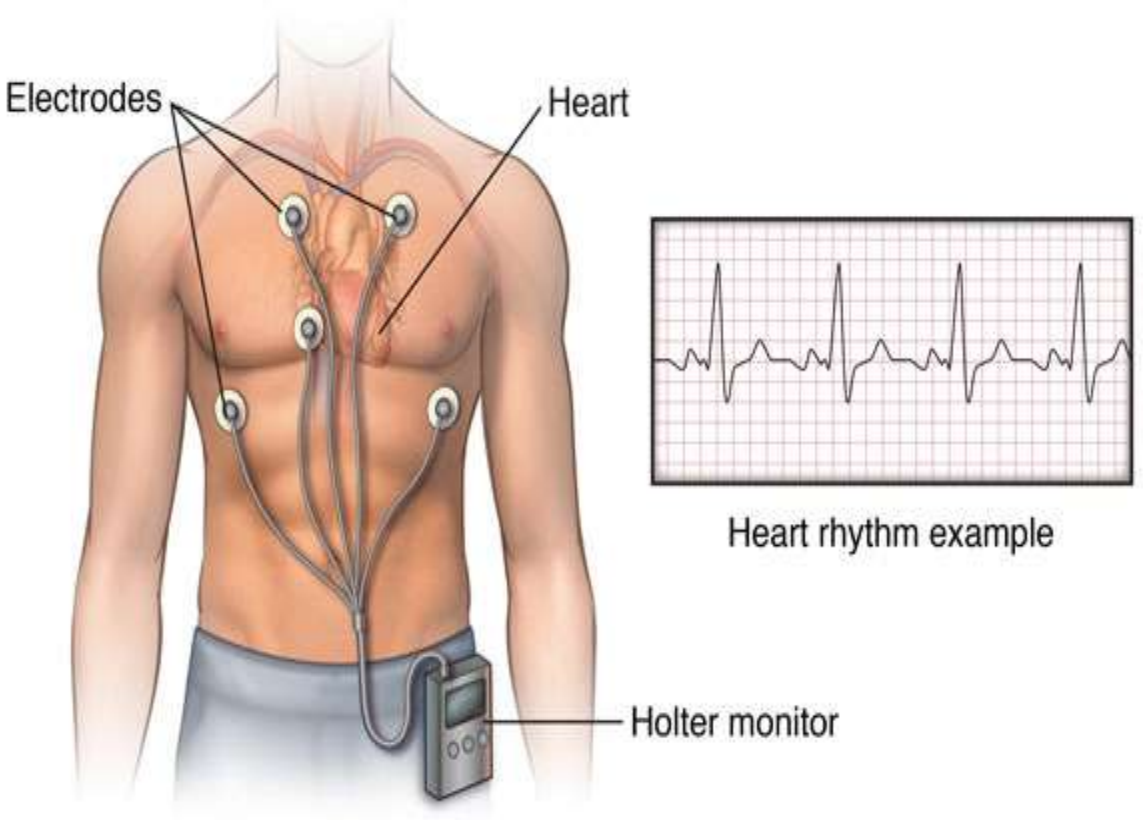

Figure 1.12 Holter monitoring test

1.7 PTB Diagnostic ECG Database

The ECG signals in this collection were collected using a prototype non-commercial PTB recorder with the following specifications:

- 16 channels (14 for ECG, 1 for respiration, 1 for mains voltage) for input
- ±16 mV Input voltage: offset voltage up to ± 300 mV compensation
- Input-resistance: 100 Ω (DC)
- Resolution: 16 bits with 0.5 micro-Volt/LSB (2000 A/D units per mV)
- Bandwidth: [0 - 1 kHz] (all channels sampling are synchronous)
- Noise: 10 μV max(pp), respectively 3 μV (RMS) with input short circuit
- Online skin registration resistance
- Recording noise level during signal acquisition

The database contains:

- 549 recordings of 290 subjects (age between 17 and 87, mean 57.2 years; 81 women, mean age 61.6 years, 209 men, mean age 55.5 years).

Each subject is represented by one to five records. There There aren't any topics numbered 124, 132, 134, or 161.

Each recording includes: 15 simultaneously signals measured: Frank's 3 ECGs (vx, vy, vz) with 12 conventional leads (i, ii, iii, avr, avl, avf, v1, v2, v3, v4, v5, v6).

Each digitized signal is 1000 samples/second, with resolution =16-bit over a range of ±16.384 mV.

Recordings are available at sample rates up to 10 KHz

- The ECG header file (extension .hea) contain a detailed clinical summary, including age, sex, diagnosis and, if applicable, data on the medical history, medications and procedures, coronary pathology, ventriculography, echocardiography and hemodynamics

- The diagnostic classes of 268 subjects are summarized below:

Table 1.1 The PTB diagnostic classes [36]

Diagnostic class	**Number of subjectc**
Myocardial infarction	148
Bundle branch block	15
Myocardial hypertrophy	7
Dysrhythmia	14
Cardiomyopathy/Heart failure	18
Myocarditis	4
Valvular heart disease	6
Healthy controls	52
Miscellaneous	4

1.8 ECG signal problems during the Acquisition

1.8.1 Reversals lead

Lead switches are a common mistake when ECGs are made and can lead to wrong diagnoses. Common mistakes are:
-Left-right arm reversals lead to a negative complex in the lead I with a negative P wave in the lead I. They are one of the most common causes of right axis deviation on the ECG!
-Arm-foot switches lead to a very small or 'far field' signal in leads II or III.
-Chest lead reversals lead to inappropriate R wave progression (increase-decreaseincrease)and are often easily recognized.
Therefore any right axis or small signal in an extremity lead should be reason enough to check lead positioning. A previous ECG can be beneficial.

1.8.2 Artifacts

Artefacts (disturbances) can have many causes. Common causes are:

-Movement
-Electrical interference

1.8.3 Filter settings

Although not a technical problem, filter settings influence the interpretation of the ECG.
To reduce electrical interference, ECG machines use two filters:
-A high pass filter reduces low-frequency noise. This filter reduces baseline drift on the ECG.
-A low pass filter reduces high-frequency noise, such as produced by chest and extremitymuscles and electrical interference from the power grid.
Depending on the purpose of the ECG these filters can be adjusted.
-In the monitor mode, the high pass filter can be set higher at 0.5-1.0 Hz and the bandstopfilter on 50 Hz. This is the most robust filter setting (the filter passes only a narrow frequency range). This setting is beneficial for rhythm monitoring, where noise can

bedistracting, and ST-segment interpretation is not very important. In this mode, pacemakerspikes are sometimes invisible while filtered out.

-In the diagnostic mode, the high-pass filter is set at 0.05 Hz and the low-pass filter at 50, 100 or 150…. Hz. This improves the diagnostic accuracy of the ST segment. However, on thedownside, a baseline drift occurs more quickly.

1.9 Conclusion

In this chapter, the idea of the cardiovascular system is introduced. This system culminates the arterial and venous circulation through the heart by its mechanical and electrical activity functions.

The preprocessing steps of the ECG signal are crucial for future segmentation and time-lapse analysis stages. Unfortunately, as we have seen, the recording conditions make the ECG noisy. Various noises associated with an ECG signal can alter clinical information to a greater or lesser extent, so it is essential to address them. In the next chapter, we will perform a detailed analysis of ECG signal noise and techniques for eliminating this noise.

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Chapter II: A Review on Biomedical ECG signal Filtering and Analysis

2.1 Introduction

The ECG signal is a potent tool in the analysis of cardiac abnormalities. Indeed, its importance is due to the effect that the P, QRS and T waves constituting this signal translate the heart's electrical activity. Therefore, a change in the shape, the duration of these waves or the duration of the different intervals between these waves can indicate the presence of a cardiac abnormality. In other words, the importance of the ECG signal is related to the clinical clues that can be extracted and used to establish a correct diagnosis.

Indeed, the extraction of these indices requires the delineation of the beginnings, peaks and ends of the different waves of the ECG signal. Therefore, manual detection of these waves is often tedious and challenging to accomplish, particularly in the case of ECG signals of the Holter type. In addition, in some cases, the analysis of the 12 leads of the ECG signal is essential to diagnose certain heart diseases better. This makes manual detection of P, QRS and T waves cumbersome. Therefore, the development of automatic detection systems is inevitable when diagnosing cardiac abnormalities from an ECG signal containing a relatively high number of heartbeats.

Several scientific works have been devoted to developing robust and reliable detection algorithms [1-3]. These algorithms generally consist of two fundamental steps. The first step is eliminating the various noises contaminating the ECG signal. In this step, it is necessary to maintain user information and not alter the different waves' shape and duration.

2.2 ECG Characteristics

2.2.1 ECG signal acquisition

The acquisition of the ECG signal is made with electrodes suitably placed on the human body

Figure 2.1 Acquisition of the electrical activity of the human heart

The acquisition chain consists of two main stages:

• A signal correction and shaping stage.

• An interfacing stage (analogue/digital conversion)

• The digital processing system (digital filtering and detection).

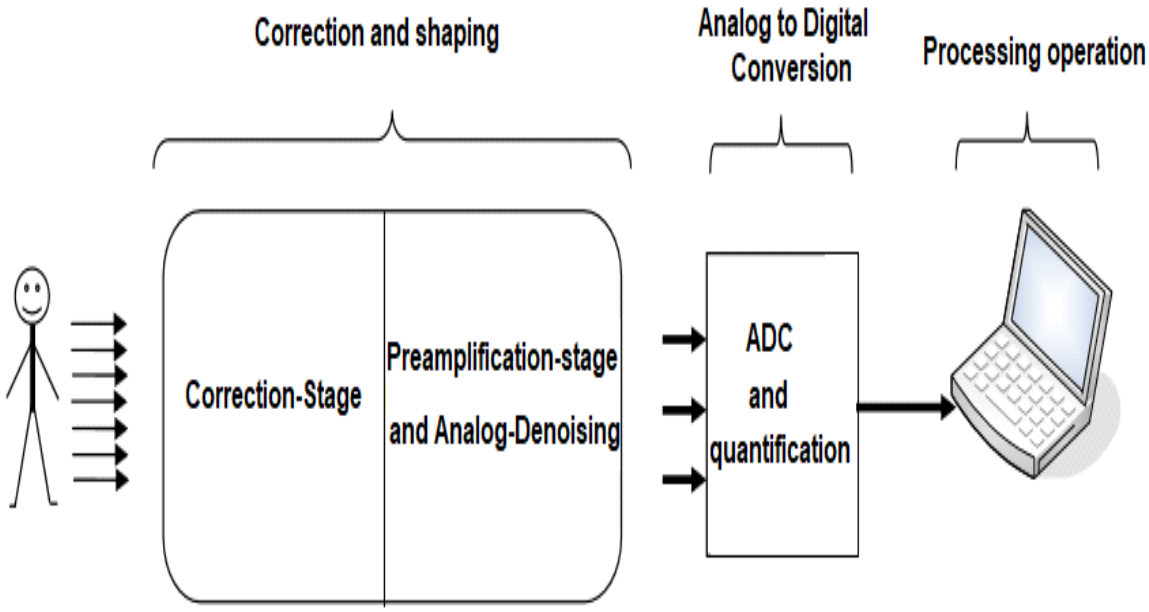

Figure 2.2 The acquisition chain

2.2.2 Non-stationarity of ECG signals

Transitions between rhythms are a non-stationary process. Non-stationarity includes the morphological properties of heartbeats and the interbeat basis: RR intervals. Thus, abnormal changes in beat morphology or rhythm are also likely. Moreover, the aetiology of these changes is often closely related [4, 5].

The dynamics of the morphological changes of the ECG signal waves could not be predicted. Some articles consider a certain periodicity [6] in the signal to apply certain algorithms, but this assumption is incorrect. Figure 2.3 shows an interval of ECG signals with arrhythmias that explain this property.

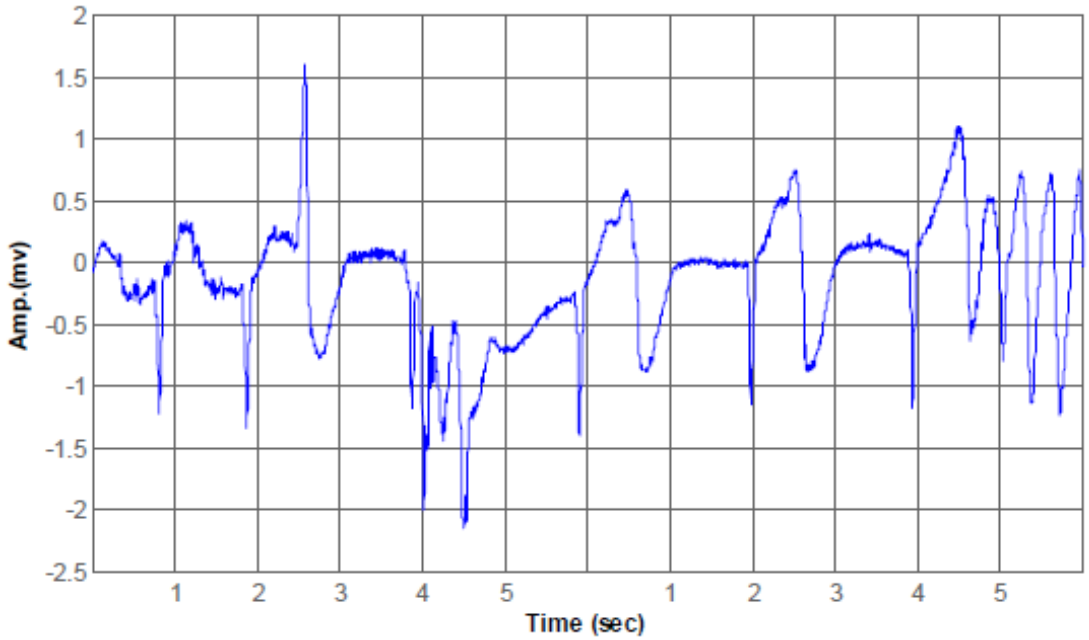

Figure 2.3 shows ECG interval with arrhythmias Changes in the morphology and heart rate have a non-stationary nature.

2.2.3 ECG Signal and Artifacts

Even with the utmost care during acquisition and recording, the ECG signal is contaminated with several unwanted signals, collectively called "artefacts". These noises are different and often cause a problem when detecting the waves of the ECG signal. Some of them are of physiological origin, i.e. generated in the human body; the others are non-physiological, i.e., external to the body. Some of these signals have an overlapping spectral band with the ECG signal itself, which means that the design of a simple bandpass filter is not evident for their elimination. The sources of artefacts are as follows:

2.2.3.1 Baseline Wander (BLW)

The baseline fluctuation means a deviation of this line from its reference value. The baseline reference value corresponds to the isoelectric segments. That is, the baseline corresponds to the PQ intervals and its fluctuation is due to patient movement, respiration

and changes in skin-electrode impedance. This type of noise is very noticeable when recording a stress ECG. It represents low-frequency noise. Indeed, this fluctuation appears as low-frequency ripples (0.15 HZ-0.3HZ).

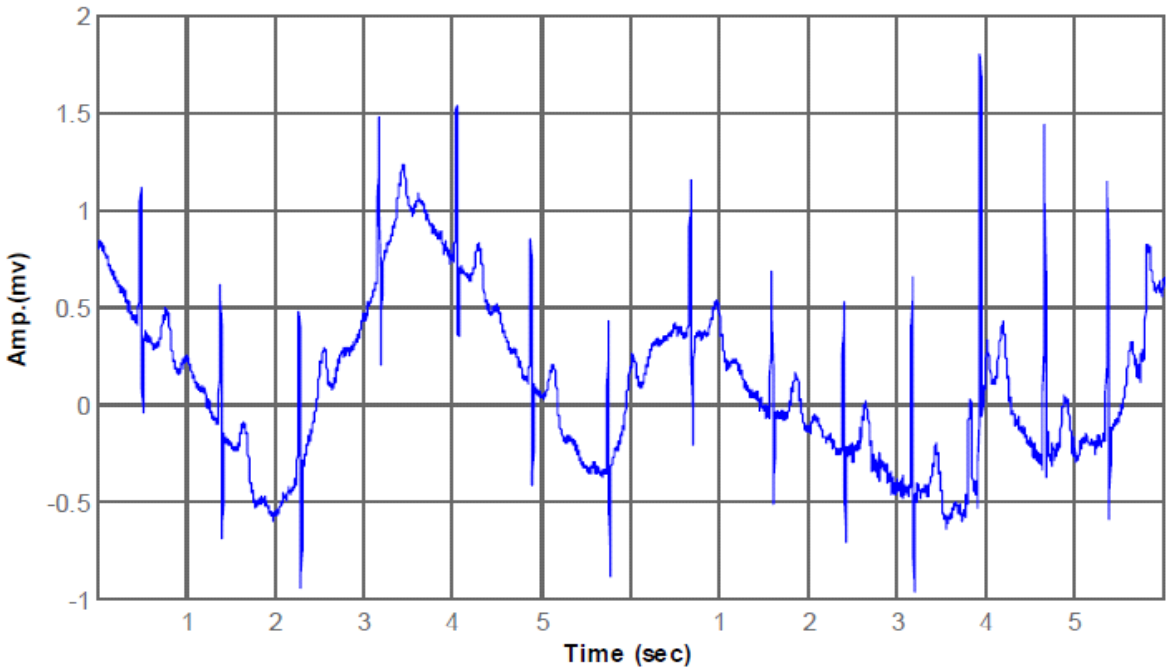

Figure 2.4 ECG signal with baseline wandering noise

2.2.3.2 Power Line interference (PLI)

This noise is the most encountered during the acquisition of the ECG signal [7]. It is due to electromagnetic interference from the distribution network. It is picked up on the conductive wires of neighbouring electric cables due to the inductive-capacitive coupling with the conductive wires of the ECG. Thus, a 50/60 ± 0.2 Hz current flows through the conductive wires to ground through the patient's body. Sometimes the equivalent voltage drop that appears as a common-mode signal at the input of the ECG amplifier can reach 20 mV, which is four times greater than the maximum ECG amplitude itself. A detailed discussion on PLI is given in [2]. A power line interference measurement technique is described in [3]. In another approach [8], line interference reduction is described where the

line reference signal is simultaneously measured, and a scaled version is subtracted from the ECG by the signal average. A selective filter is often used to eliminate this type of noise.

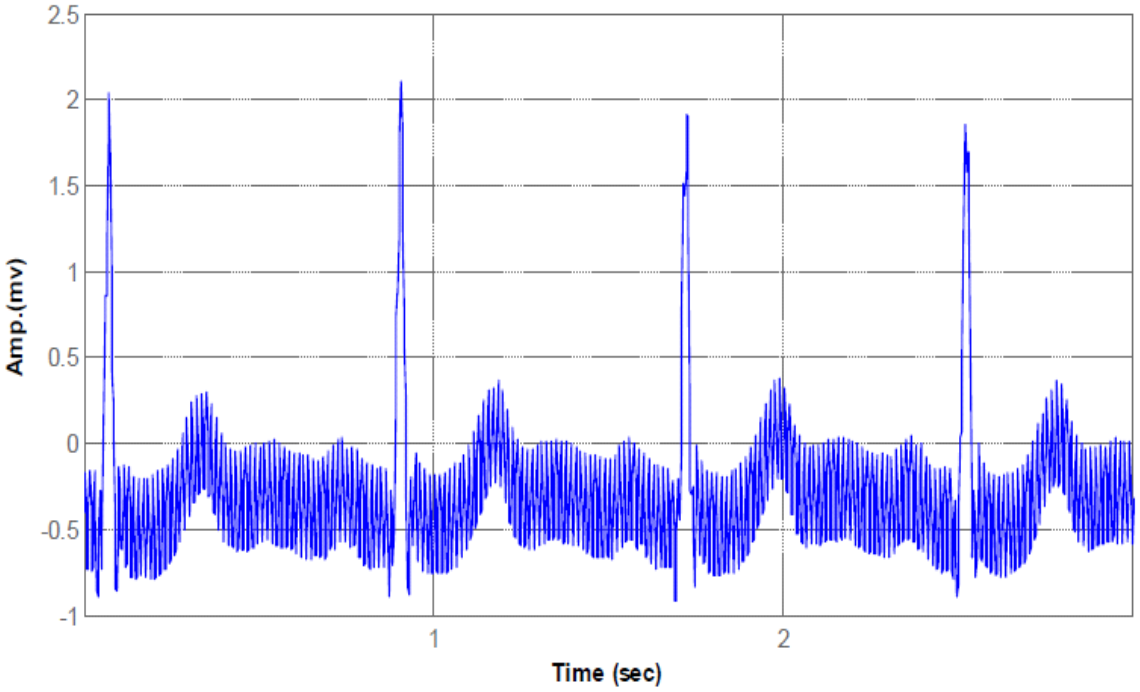

Figure 2.5 Nominal 50 Hz frequency Power line interference added to ECG signal

2.2.3.3 Electromyography (EMG) noise

EMG signals are captured signals that translate the electrical activity of the patient's muscles (cells located outside the target organ). Their amplitude is between 0.1–1 mV, and their frequency band is 5 Hz–1 kHz (> 100 Hz), which partially overlaps the ECG signal. Their elimination is done by using low-pass filters.

This noise can destroy the analysis if not correctly handled. For clinical tests of short duration, the patient is advised to lie down at rest to minimize this noise. However, for long-term Holter monitoring, this EMG noise is unavoidable.

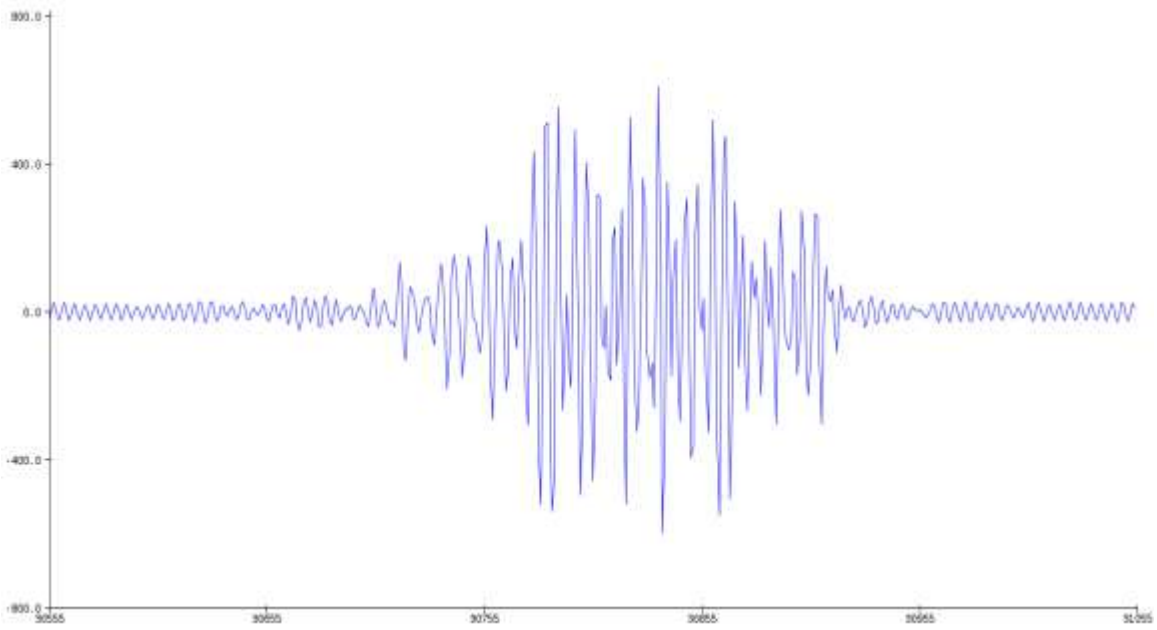

Figure 2.6 electromyography (EMG) signals

2.2.4 Other artifacts

2.2.4.1 Motion Artifacts:

Patient movement is the most common source of artifacts. It significantly overlaps with the spectrum of the ECG signal in the band from 1 to 10 Hz. As a result, a sharp jump or a complete baseline saturation appears at the amplifier's output for 0.5 s. We distinguish:

- Random movements, causing image blurring with diffuse noise, propagated in the phase encoding direction.
- Periodic movements at the origin of ghost images propagated according to the phase encoding direction.

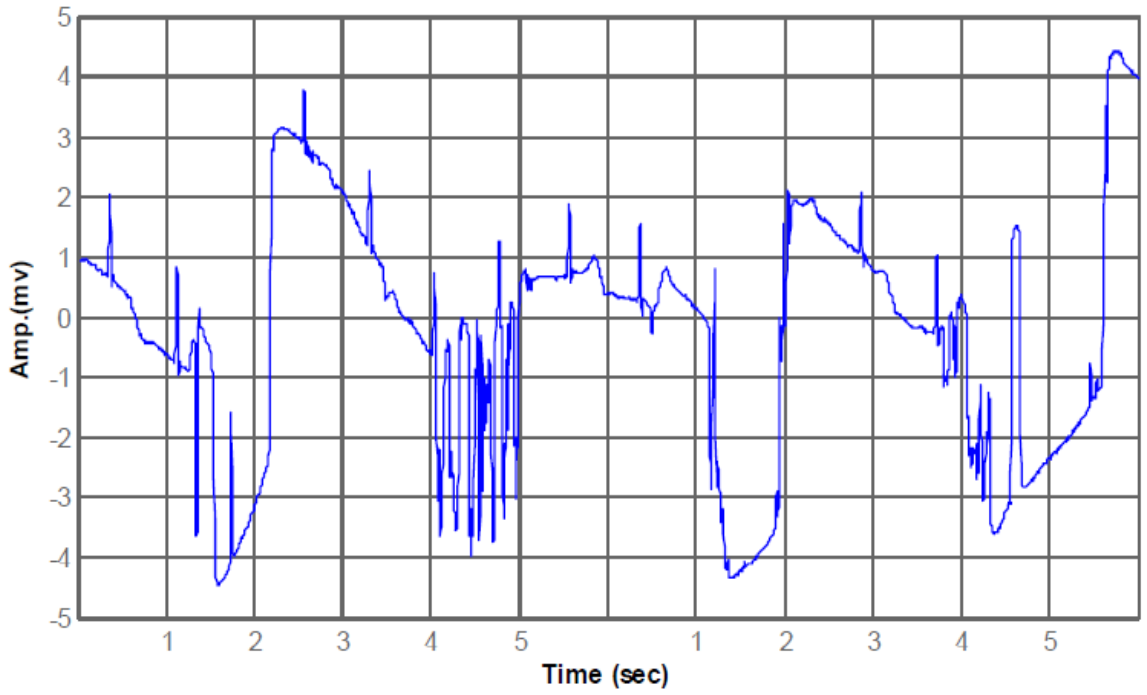

Figure 2.7 Motion artefacts contaminating the ECG signal

2.2.4.2 Electrode pop or contact noise

Sometimes loss of contact between the patient skin and electrode may cause a temporary saturation of the amplifier output for a certain period.

2.2.4.3 Electrosurgical noise

This is the noise neighboring medical equipment generates in the clinical setup at frequencies between 100 kHz and 1 MHz.

2.2.4.4 Amplifier noise

Noise and drift are two unwanted signals that are generated within the amplifier that contaminate a bio-potential signal under measurement. 'Noise' generally refers to undesirable signals with spectral components above 0.1 Hz, while 'drift' refers typically to slow changes in the baseline at frequencies below 0.1 Hz. The noise and drift are measured

either in microvolts peak to peak (lVp-p) or in microvolts root mean square (RMS) (lVRMS) and appear as if they were applied as differential input voltage.

2.2.4.5 Quantization noise

The AD converter, having a finite bit width, samples the amplified ECG to generate a sequence of discrete data, digitized representations approximated to the nearest bit. Quantization noise thus refers to this truncation of the analogue samples, which are of infinite resolution, to a binary number of finite width and equal to ±1 LSB of the AD converter.

A detailed discussion on ECG artifacts can be found in [7-9]. Suitable designs and clinical setup can minimize these artefacts; however, it is impossible to eliminate those altogether using hardware designs completely. Nowadays, many soft computational techniques are available for denoising digitized ECG.

2.5 Motivation of filtering

The optimal performance of an ECG filtering algorithm depends primarily on the ability to separate the signal from artifacts and the amount and nature of the distortion introduced by the filter. In addition, apost-filtering step is essential to reduce signal distortion. Both guidelines are pretty challenging to assess because the diagnosis is subjective and depends on the shape of the ECG signal. The most crucial task in ECG signal processing is accurately detecting QRS complexes. All subsequent processing steps are based on the position of the QRS waves as the essential information. Unfortunately and as already mentioned, the recorded ECG is often disturbed by different types of noise. Data corrupted by noise must be pre-filtered or deleted. Therefore, ECG quality assurance requires both human and artificial noise detection schemes so as not to lose clinically important information.

During ECG recording, noise can only be reduced but not eliminated, so it is vital to use a method with good noise sensitivity. ECG filtering algorithms usually contain a centre band pass filter in the range [11 - 16 Hz]. After passing through the filter, the signal can be

squared or averaged over some samples to obtain the square of the QRS waves. Unfortunately, these static techniques suffer from two significant problems:

- The QRS waveform varies from patient to patient and depends on the patient's condition;
- Complex noise and QRS bandwidths overlap.

The non-linear behavior of the human body implies that all processing methods must be able during the measurement to change state. Otherwise, they introduce a considerable amount of artificial noise. Designing an optimal matched filter can increase the signal-to-noise ratio (SNR). Still, the non-stationary nature of the signal and noise involved in the measured ECG hinders the practicality of these filters for QRS detection. A linear filter cannot effectively whiten noise from a non-linear ECG signal.

Artificial neural networks are inherently non-linear models, so ANN-based filtering is potentially useful. In the case of a complex and strongly non-linear behavior signal, like almost all biological signals, we should use two hidden layers, which generally provide good approximation results and simultaneously allow a good speed of learning and adaptation. In practice, the ANN model can fit much better than linear models. The number of input units corresponds to the order of the filter, which should not be increased too much to allow good transient properties permanently. After the preprocessing, filtering, evaluation and estimation of the model parameters, a reconstruction of the signal is necessary. At this point, the post-filtering algorithm "knows" the key ECG-specific information, allowing it to better separate any man-made noise from the signal. The application of ECG and patient-dependent information is necessary to develop a successful filter. This problem can only be solved if the computer knows about the formation of the ECG signal.

Artificial neural networks (ANN) are applied in several interesting biomedical applications in data processing [10]. The best-known neural solutions involve multilayer perceptrons, self-organized Kohonen networks, fuzzy or neuro-fuzzy systems, genetic algorithms, and combining different solutions within a hybrid system [11].

A complex ECG analyzer applies many neural networks and chooses the best while discarding the rest. The most efficient approaches are usually based on combining many classifiers using either different classifier network structures or data preprocessing methods [12]. The support vector machine (SVM), pioneered by [13], and had to solve the

main drawbacks of conventional artificial neural networks, such as:

- Modern biological problems are high-dimensional, and if the underlying mapping is not very smooth, the linear paradigm needs an exponentially increasing number of terms with increasing dimensionality of the input space, which means an increase in the number of independent variables. This is called "the curse of dimensionality".
- The fundamental data generation laws can generally be far from the normal distribution, and a model builder must manage this difference to build an efficient learning algorithm;
- The maximum likelihood estimator (and therefore the sum of the squared error cost function) should be replaced by a new uniformly better induction paradigm to properly model non-Gaussian distributions.
-

SVM classifiers have become very popular due to their robustness and stability [14]. An SVM used in an ECG parameter extraction and processing system is rigorously based on statistical learning theory and simultaneously minimizes training and testing errors. They produce a unique and globally optimal solution and are widely used in various applications, including medical diagnostics [15].

2.6 De-noising Techniques

During the pre-processing stage, the main objective is to filter the useful signals from unwanted noise. In electrocardiography, these noises are well identified, but some have the particularity of overlapping with the spectral band of the ECG, which sometimes makes them difficult to filter.

We will introduce in this part some key methods quoted in the literature; then we will present the pre-processings that we have studied in our work for the characterization of heartbeats.

Several techniques have been developed to eliminate artefacts that contaminate the ECG signal. Most of these works used adaptive filters or Infinite Impulse Response (IIR) filters by choosing a bandwidth relative to the information sought [16][17]. Chouhan et al. [18]

proposed an averaging filter for filtering the ECG signal. In this technique, the average of the ECG signal is subtracted from the signal beforehand. Then a fifth-order polynomial is applied to obtain a baseline estimate which will then be removed from the ECG signal. Shusterman et al. chose to use an algorithm based on multi-rate filter banks. This algorithm makes it possible to avoid the problems of phase shifts and minimization of the calculation time compared to a single filter. However, since the ECG signal is a signal that contains several spectral components, it is also non-stationary and often affected by noise correlated to the signal, such as muscle artefacts. Most recent works use filtering based on the wavelet transform [19, 17].

In general, the ECG de-noising techniques can be classified into one of the following categories:

- Wavelet methods;
- Digital filtering techniques adaptive and non-adaptive;
- Source separation methods principal component analysis (PCA) and independentcomponent analysis (ICA);
- Neural networks filtering;

The standard performance parameters used for noise removal from the ECG are given as:

- Minimum Mean Square Error (MMSE): Indicates how well the system performs its filtering task.

A low MMSE indicates that the adaptive system has "converged" to the desired solution. Parameters that affect this criterion are but are not limited to: the order of the adaptive system, the quantization error and the measurement noise. The excess root means square error (exceeding MSE) is defined as the difference between the actual root mean square error (MSE) at the adaptive filter output and what it should be if the adaptive filter coefficients were kept at their optimal values.

$$MSE = \frac{1}{N}\sum_{i=1}^{N}[x(i) - x^{\sim}(i)]^2 \quad (2.1)$$

- The adjustment error (misadjustment) essentially depends on:

- Gradient noise.
- The sensitivity of the coefficients to the quantization effect (distortion).
- The order of the adaptive filter.
- The amplitude (magnitude) of the measurement noise.

- Accuracy of the estimation of the filter parameters:

The precision of the assessment of the filter coefficients is rather important insofar as it allows acceptable conditions of the adjustment error.

- Signal to Noise Ratio:

$$\text{SNR}=10\times log\frac{\sum x^2(i)}{\sum n^2(i)} \quad (2.2)$$

- Percentage Root Mean Square Difference:

$$PRD = \sqrt{\frac{\sum_{i=1}^{N}[x(i)-x^{\sim}(i)]^2}{\sum n^2(i)}} \quad (2.3)$$

Where N is the total number of samples, x is the clean sample, n is the known noise, and ~x is the denoised sample. Some authors have also estimated a few indirect measures, viz.,

percentage noise retention ratio (PNR) [20], noise reduction factors (NRF) [21], and SNR improvement defined as:

- Percentage Noise Retention:

$$PNR = \frac{P_{ds} - P_{es}}{P_{es}} \times 100 \quad (2.4)$$

- Noise Reduction Factor :

$$PRD = \sqrt{\frac{\sum_{i=1}^{N}[x(i) - x^{\sim}(i)]^2}{\sum_{i=1}^{N}[x^{\wedge}(i) - x(i)]^2}} \quad (2.5)$$

- SNR improvement (SNR imp) [dB] :

$$(SNR\ imp)[dB] = SNR_i - SNR_0 = 10 \times log \frac{\sum \frac{x^2(i)}{n^2(i)}}{\sum \frac{x^2(i)}{[x^{\wedge}(i) - x(i)]^2}} \quad (2.6)$$

Where$P = 10 \times log \sum_{i=1}^{N}[x(i)]^2$; *Pes* denotes the power of the clean signal, and *PDS* is the same as the denoised signal, x^ is the composite (noisy) signal with the clean ECG, $x^{\sim}(i) - x(i)$is the residual noise. *SNRi* and *SNRo* , respectively, denote the *SNR* at input and output.

In the rest of this chapter, we will study some filtering approaches.

2.6.1 Wavelet Transform

The Fourier transform (TF) is a mathematical transformation that allows passing from the time domain to the frequency domain. It can be applied to non-stationary signals such as bioelectrical signals (ECG, EEG, EMG, etc.). Still, it is ideal for stationary signals whose frequency properties do not vary over time. It is for this reason that the wavelet transform is preferred.

Wavelet transforms methods that analyze the content of a signal concerning its frequency. These time-scale approaches allow the decomposition of a signal and its study in the different frequency bands. In this case, a window called the mother wavelet, whose width is variable. Their goal is to obtain more precision in the results depending on the type of frequencies (high or low)

With

$$\mathrm{T(a,b)} = \int f(t)\beta a, b(t)dt \qquad (2.7)$$

The wavelet coefficients T (a,b) depend on two parameters, a and b, where a is the scale factor, and b is the translation factor. The functions are obtained from the dilation and translation of the parent wavelet function.

We will not go into the theoretical and mathematical foundations of the construction of wavelets because their details are profound.

Wavelet transforms divided into two categories:

Continuous Wavelet Transform (CWT) and Discrete Wavelet Transform (DWT) the main difference between these two categories is that the CWT operates on all continuous values of frequency and time. While DWT operates on a subset defined specifically over the set of all discrete frequency and time values [22].

One of the advantages of wavelets is their remarkable ability to support several digital signal processing almost simultaneously (windowing - denoising detection filtering and

signal reconstruction) [23].

Generally, the wavelet transform is performed in three successive steps:

- The application of the wavelet transforms to the signal affected by the noise.
- The filtering of the coefficients thus obtained, following a specific criterion (by thresholding).
- The calculation of the inverse transform, from the coefficients resulting from the previous step.

And according to [24], the wavelet transformation's effect shows that the latter's filtering makes it possible to reduce the derivative of the baseline of the ECG signal.

This approach aims to make a new method of beat-to-beat cancellation of the QRS-T to facilitate the detection of the P wave. The phase of this cancellation is based on wavelet decomposition of the ECG signal, observed on two leads (ECG1 and ECG2), in order to provide a residual signal which must contain only the P wave train after reconstruction by the wavelets Figure 2.8.

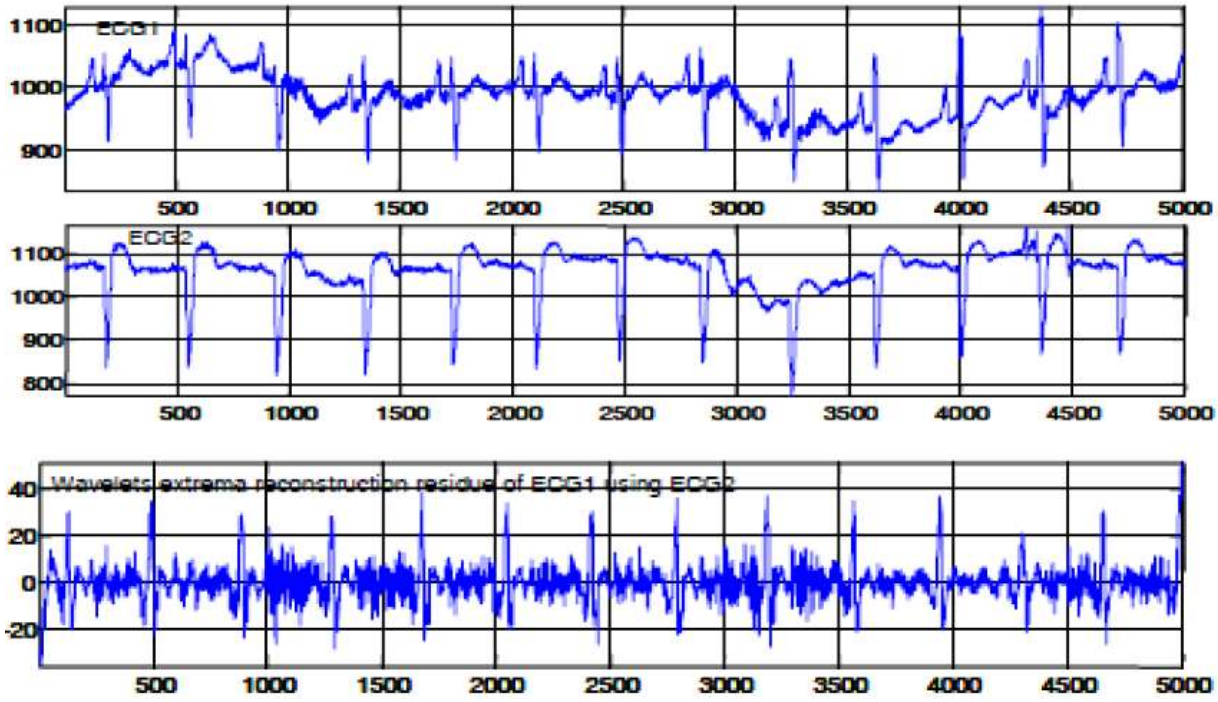

Figure 2.8 Baseline derivative reductions by wavelet filtering.

2.6.1.1 Decomposition of the singular value

The singular value decomposition is the most general decomposition for matrices, and it can be applied to any matrix with it; one can, for example, calculate inverses and make data reduction. Moreover, any actual, complex, square or rectangular matrix can be transformed into a diagonal matrix Σ by orthogonal transformations and [25]. Hence, this decomposition is known as the singular value decomposition.

The SVD decomposition of a matrix A:

$$A= UWV^T$$

$$V= [v_1\, v_2 \ldots\ldots\ldots\ldots v_n]$$

$$U= [u_1\, u_2 \ldots\ldots\ldots\ldots u_n]$$

Due to the energy-conserving orthogonal transform in the SVD, these subspaces correspond to the characteristics of the signal and noise contained in the data [26]. To filter out the noise and other unfavourable signal characteristics, we project the data onto the desired subspace by simply setting all corresponding singular values in the SVD spectrum of the data to zero. The estimate of the ECG signal is then recovered from its projection.

2.6.2 Adaptive filtering

Adaptive filtering involves the change of filter parameters (coefficients) over time. It adapts to the change in signal characteristics to minimize the error. It finds its application in adaptive noise cancellation, system identification, frequency tracking and channel equalization [27]. Figure 2.9 shows the general structure of an adaptive filter.

Adaptive filtering is used when it is necessary to create, simulate or model a system whose characteristics change over time. It leads to the implementation of time-varying coefficient filters. The variations of the coefficients are defined by an optimization criterion and carried out according to an adaptation algorithm, which is determined according to the

application [28]. Adaptive filtering techniques find their full meaning in problems for which the noise component or the process has a strange spectral behaviour. In the case, for example, of a signal disturbed by a sinusoidal parasite at a frequency of 50Hz, the filtering is effective when using a conventional band-stop filter centred on 50Hz. On the other hand, in the case of the measurement on the electrocardiogram of the heart rate of a baby still in the womb of its mother, the signal will be parasitized by the mother's heart rate. This spurious signal is a priori of unknown spectral content and even risks being partially superimposed on the signal corresponding to the baby. Conventional filtering is therefore inefficient here, whereas adaptive filtering will be effective [29].

There are four classes of applications:

- Identification: This consists of determining a filter that best models the behaviour of an unknown process.

  Only the input/output signals of this process are known. Therefore, the filter representing the model will be estimated from observing the difference between the output of the process and its estimate at the output of the filter.
- Prediction: This problem consists of estimating the future value of a signal from past information. Predict the future state, or anticipate the future evolution of a quantity to make a decision as quickly as possible.
- Interference cancellation: Adaptive filtering will compensate for the influence of the parasite on the electrocardiogram (the mother's electrocardiogram "parasite" the baby's electrocardiogram useful signal).
- Inverse modelling: This involves reconstructing a reference signal that an unknown process has deformed as best as possible. The adaptive filter must allow compensation of the deformations induced by the process. In Telecom, this problem is referred to as an equalization problem [28].

The development of adaptive filtering was born from the rise of digital processing, the sustained growth in the power of processing processors, which allow the implementation in real-time, increasingly complex algorithms and which go increasingly high Adaptive methods in signal processing aim to:

By the way the adaptation of processing tools to the statistical properties of signals and systems, as well as adaptation to their fluctuations over time.It is, therefore, a well-balanced mixture between stationarity and non-stationarity.

Stationarity makes it possible to permanently maintain, over time, the statistical properties, thanks to which purely random fluctuations are eliminated or at least reduced. Conversely, non-stationarity is the slow or rapid variation over time of statistical properties, without which there would be no need for adaptation.

The optimal filter could be calculated only once without fluctuating signals and systems. Therefore, filters can be classified as linear or non-linear [30].

2.6.2.1 Diagram

The idea behind a closed-loop adaptive filter is that a variable filter is adjusted until the error (the difference between the filter output and the desired signal) is minimized. The least Mean Squares (LMS) filter and Recursive Least Squares (RLS) filter are types of adaptive filters.

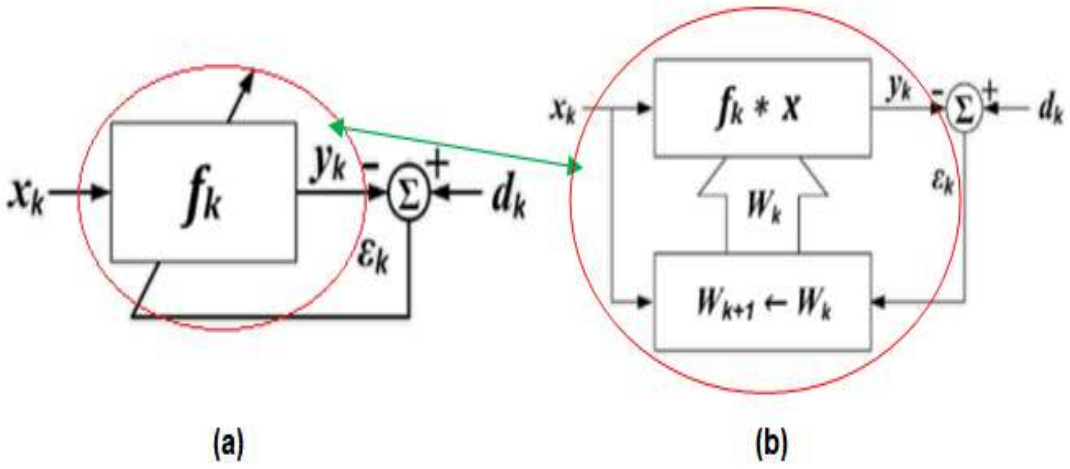

Figure 2.9 Adaptive-filter structure (a): linear filter structure (b): adaptation algorithm

k is sample number, *x* is reference input, *X* is the set of recent values of *x*, *d* is desired input, *W* is the set of filter coefficients, ε is error output, f is the impulse response of the filter, (*) is the convolution operator, Σ represents the summation,

The adaptive filter has two input signals: *dk* and *xk* sometimes called primary input and reference input, respectively. [31] The adaptation algorithm filters the reference input into a replica of the desired input by minimizing the residual signal, epsilon *εk*. When the adaptation is successful, the output of the *yk* filter is effectively an estimate of the desired signal.

dk which includes the desired signal plus unwanted interference and *xk* which includes signals that are correlated with some of the unwanted interference in *dk*.

k represents the discrete sample number.

The filter is controlled by a set of *n+1* coefficients or weights.

$Wk = [w1k\ w2k \ldots\ldots\ldots\ldots wnk]T$ represents the set or vector of weights, which controls the filter at sampling time *k*.

where *wnk* refers to the nth weight at the k^{th} time.

Wk represents the change in weights that occurs as a result of adjustments calculated at sample time *k*.

These changes will be applied after sample time k and before they are used at sample time *k+1*.

The output is usually *εk* but it could be *yk* or it could even be the filter coefficients. [32]

For example, the recording of a heartbeat (an ECG) can be altered by mains noise. The exact frequency of the power and its harmonics can vary from moment to moment.

One way to suppress the noise is to filter the signal with a notch filter at and near the mains frequency, but this could excessively degrade the quality of the ECG because the heartbeat would also likely have frequency components in the discarded range.

To circumvent this potential loss of information, an adaptive filter could be used. The adaptive filter would take input from both the patient and the mains and thus be able to track the actual frequency of the noise as it fluctuates and subtracts the noise from the recording. In addition, such an adaptive technique generally allows having a filter with a smaller rejection range, which means, in this case, that the quality of the output signal is more accurate for medical purposes [33], [34].

2.6.2.2 Adaptive Algorithms

In adaptive filters, the weight vectors are streamlined by an adaptive algorithm to minimize the cost function. The algorithms used by us for noise reduction in ECG in this thesis are least mean square (LMS), Regularized least mean square (NLMS), sign data least mean square (SDLMS), sign error least mean square (SELMS) and sign-sign least mean square (SSLMS) algorithms [35].

The choice of the algorithm will be made according to the following criteria:

- The convergence speed will be the number of iterations necessary to converge "close enough" to the optimal solution.
- The measurement of this "proximity" between this optimal solution and the solution obtained.
- The ability to track variations (non-stationarities) of the system.

  • Robustness to noise.
  • The complexity.
  • The structure (modularity, parallelism, ...).
  • The numerical properties (stability and precision) in the case of a limited precision on the data and the filter coefficients. [36]

2.7 Digital filtering

A digital filter is an element that performs filtering using a succession of mathematical operations on a signal, that is to say, it modifies the spectral content of the input signal by attenuating or eliminating certain unwanted spectral components.

Unlike analogue filters, which are made using an arrangement of physical components (resistor, capacitor, etc.), digital filters are made either by dedicated integrated circuits, programmable processors (microprocessor, microcontroller, etc.) or by software in a computer.

There are two leading families of linear digital filters: Infinite Impulse Response (IIR) filter. This filter is characterized by a response based on the input signal's values and the previous values of this same response. It is so named because the impulse response of this type of filter is theoretically infinite in duration. It is also referred to as a recursive filter. The other type is the Finite Impulse Response filter (FIR filter). Unlike the IIR filter, the response of the FIR filter only depends on the values of the input signal. Therefore, the impulse response of an FIR filter is always of finite duration.

This digital filtering eliminates high-frequency signals secondary to muscle activity other than the heart and interference from electrical devices [37].

In our work, the type of filter used is infinite impulse response (IIR), Butterworth type.

2.7.1 FIR and IIR filtering

Digital filters are classified either as Finite Impulse Response (FIR) filters or Infinite Impulse Response (IIR) filters, depending on the form of unit pulse response of the system. In the FIR system, the impulse response is of finite duration, whereas, in the IIR system, the impulse response is of infinite duration. IIR filters are usually implemented using structures having feedback, that's why the present response of the IIR filter is a function of present and past values of the excitation as well as the past value of the response.

But the response of the FIR filter is usually implemented using structures having no feedback, so the response depends only on the present and past values of the input only [38].

The design of FIR filters is preferred due to the following advantages:

- Always stable
- Exact linear phase
- Design methods are linear
- Can be realized efficiently in hardware
- Filter start-up transients have a finite duration

2.7.1.1 Structure of the IIR filter

Infinite impulse response (IIR) filters are types of electronic filters, also called recursive filters, by the presence of recursion. The output signal of the filter is fed back into the input of the filter, constituting a recursive circuit (figure 2.10). This method makes it possible to produce filters with a more complex response with fewer data. As energy is constantly fed back into the circuit, the impulse response has an infinite potential duration, hence the name given to these filters.

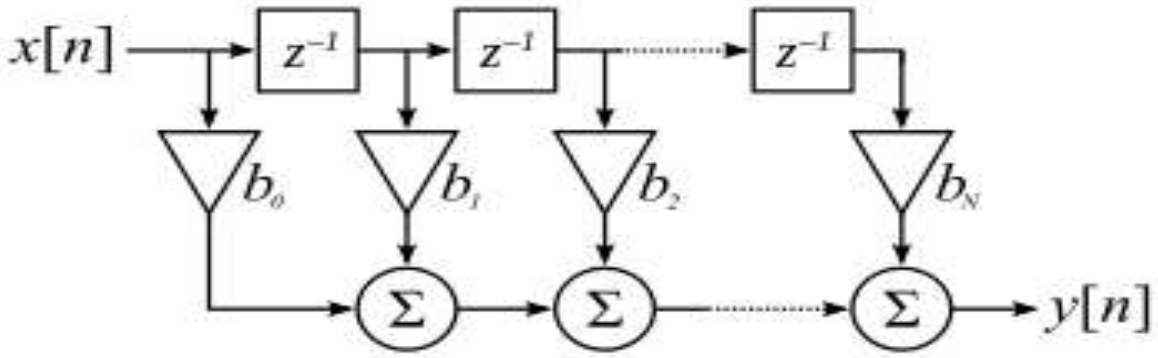

Figure 2.10 IIR filter operation

2.7.2 FIR Filters Design Techniques

The approach is similar to designing a filter analog:

- Filter specification

- Calculation of coefficients
- Choosing an implementation architecture
- Simulation (optional if you are sure of yourself)
- Implementation

To ensure stable filter functioning, FIR filters are implemented non-recursively. The design of the FIR filter consists of two essential parts

- Approximation stage
- Realization stage

In the approximation step, the filter's specifications are taken, and a transfer function is generated. First, the ideal frequency response and the FIR filter order N of are taken in this case. Then, an algorithm is selected for setting up the filter transfer function.

The realization part consists in choosing the filter structure (diagram, circuit or program) to implement the transfer function.

The three best-known methods for designing FIR filters are:

- Window method, which makes the approximation of *h(n)*by the truncated inverse Fourier the amplitude spectrum $H(\omega)$
- A sampling of the amplitude spectrum followed by the reverse Fourier transform*H(ω)*
- The method of equal undulations of Parks- McClellan

In the completed work (last chapter), we adopted the FIR filter design window method for noise reduction.So,the window method of filter design is discussed in the following section.

2.7.2.1 FIR Filter Design Based on Window

In this process, the desired frequency response specification $Hd(\omega)$ and the corresponding unit sample response $hd(n)$ are determined using the inverse Fourier transform (IFT).

The relationship between $Hd(\omega)$ and $hd(n)$ is done by:

$$H_d(\omega) = \sum_{i=0}^{\infty} h_d(n) e^{-j\omega i} \quad (2.7)$$

Where

$$h_d(\omega) = \int_{-\pi}^{\pi} H_d(\omega) e^{j\omega i} \quad (2.8)$$

The *hd* (*n*) impulse response obtained from Eq. 2.8 is of infinite duration. So, it is truncated at some point, say n = *M* - 1 to yield an FIR filter of length *M* (i.e. 0 to *M*-1). This truncation of *hd(n)* to length *M* - 1 is done by multiplying *hd(n)* with a window. Here the design is explained by considering the (rectangular window), defined as:

$$w(n) = \begin{cases} 1 & n = 0, 1, 2 \dots \dots . M - 1 \\ 0 & otherwise \end{cases} \quad (2.9)$$

Thus, the impulse response of the FIR filter becomes as.

$$h(n) = h_d(n) w(n) = \begin{cases} h_d(n) & n = 0, 1, 2 \dots \dots . M - 1 \\ 0 & otherwise \end{cases} \quad (2.10)$$

Now, the window function *w*(*n*) with *hd*(*n*)multiplication is equivalent to *Hd(ω)* with *W(ω)*, convolution product, where *W(ω)* is the window function Fourier frequency transform domain.

$$W(\omega) = \sum_{i=0}^{\infty} w(n) e^{-jwn} \quad (2.11)$$

Thus, the$Hd(\omega)$ with $W(\omega)$convolution yields the frequency response of the truncated FIR Filter *H (ω).*

$$H(\omega) = \frac{1}{2\pi}\int_{-\pi}^{\pi} H_d(v)W(\omega - v)dv \qquad (2.12)$$

The frequency response can be obtained by $h(n)$Fourier transform:

$$H(\omega) = \sum_{i=0}^{\infty} h(n)e^{-j\omega n} \qquad (2.13)$$

But direct Fourier series $hd(n)$ to M terms to obtain $h(n)$ truncation is known to introduce ripples in the frequency response characteristic $H(\omega)$. It is due to the non-uniform convergence of the Fourier series at a discontinuity. The Oscillatory behavior near the band edge of the filter is called the Gibbs phenomenon.
Thus, the frequency response using Eq. 2.13 contains ripples in the frequency domain [39].

To reduce the ripples, $hd(n)$ is multiplied with a window function that contains a taper and decays toward zero gradually instead of abruptly as it occurs in a rectangular window. As $hd(n)$ and $w(n)$ sequences, multiplication in the time domain is equivalent to $Hd(\omega)$ and $W(\omega)$ convolution in the frequency domain, it has the effect of smoothing $Hd(\omega)$.

The several effects of windowing the Fourier coefficients on the frequency response of the filter are as follows [40]:

- A significant effect is the discontinuities in$Hd(\omega)$.
- Transition bands width t depends on the width of the main lobe of the window function frequency response $w(n)$ i.e. $W(\omega)$.
- Since the filter frequency response is obtained via a convolution relation, it is clear that the resulting filters are never optimal.

- As *M* (the length of the window function) increases, the main lobe width of $W(\omega)$ is reduced w, reducing the width of the transition band, but this also introduces more ripple in the frequency response.
- The window function eliminates the ringing effects at the band edge and results in lower side lobes at the expense of an increase in the width of the filter's transition band.

The advantages of using the window method are its ease of use and relative simplicity compared to other methods. However, the success of the window method lies in the fact that well-defined equations are often available to calculate the window coefficients.
Unfortunately, there are problems in the design of filters using the window method [41]:

- This method is applicable only if $Hd(\omega)$ is integrable, i.e. only if Eq. 2.13 can be evaluated. When $Hd(\omega)$ is complicated or cannot easily be put into a closed-form mathematical expression, the evaluation of $hd(n)$ becomes problematic.
- The use of windows allows very little design flexibility. Generally, in low-pass filter (LPF) design, the pass-band edge frequency cannot be specified exactly, since the window smears the discontinuity in frequency. Thus, the ideal LPFwith cut-off frequency *fc* is smeared by the window to give a frequency response with pass-band cut off frequency $f1$ and stop-band cut-off frequency $f2$.
- The window method is used to design prototype filters like low pass, high pass, band-pass, etc. However, this limits its applications [39], [42].
  There are different types of windows presented, such as.

- Rectangular-window

$$W_R(\mathrm{n})=\begin{cases}1 & 0 \le n \le M-1 \\ 0 & otherwise\end{cases} \qquad (2.14)$$

- Hanning-window

$$W_{hn}(\mathrm{n})=\begin{cases}0.5-0.5*\cos(\frac{2\pi n}{M-1}) & 0\le n\le M-1\\ 0 & otherwise\end{cases} \quad (2.15)$$

- Hamming-window

$$W_{hn}(\mathrm{n})=\begin{cases}0.54-0.46*\cos(\frac{2\pi n}{M-1}) & 0\le n\le M-1\\ 0 & otherwise\end{cases} \quad (2.16)$$

- Blackman-window

$$W_{hn}(\mathrm{n})=\begin{cases}0.42-0.5*\cos(\frac{2\pi n}{M-1}) & 0\le n\le M-1\\ 0 & otherwise\end{cases} \quad (2.17)$$

The windows used in our work to design FIR filters are mentioned in chapter 4 of this thesis.

2.8 Conclusion

The ECG is a powerful tool for detecting cardiovascular disease. Due to the many noise sources, this signal must be distorted and presented in a clear waveform. Noise sources can be interference from power lines, external electromagnetic fields, random body

movements, or breathing. In this chapter, several noise reduction methods are presented concerning the approximation and realization algorithms for digital filters and the window-based FIR filter design techniques, which are the focus of the newly published contributions. We will provide extensive details in the last chapter of this thesis.

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Chapter III: SoC platforms based on programmable circuits

3.1 Introduction

A system on a chip is the integration of a complete system on a single piece of silicon. This term has become very popular in the industry despite the lack of a standard definition [1]. Some consider a complex circuit to make it a System on Chip (SoC) automatically, but that would likely include every circuit in existence today. A more appropriate definition of a system on the chip would be: "a complete system on a single piece of silicon, resulting from the coexistence on silicon of numerous functions already complex in themselves: processor, digital signal processing (DSP), memories, buses, converters, analogue blocks, etc. it must have at least one software processing unit (a CPU) and must not depend on any (or very few) external components to perform its task. As a result, it requires both hardware and software.

The field of chip design for different systems, such as integrated circuits for specific applications, general-purpose processors or evenDSP processors, presents many challenges, as stated by the International Semiconductor Technology Roadmap. Among these, the problem of the gaps between productivity growth, verification of system engineers, and the number of components to be integrated into architecture remains a major research effort in this field of applications.

There are several reasons why the single-chip solution is an attractive way to implement a system. Today's manufacturing processes allow logic and memory to be combined on a single chip, reducing the overall memory access time. Since the application's memory requirement does not exceed the on-chip memory size, memory latency will be reduced by eliminating data traffic between separate chips. The number of pins can also be reduced. These characteristics, combined with low consumption and short design time, allow more economical and practical products to be quickly put on the market.

For example, we find two types of system-on-chip design technologies, ASIC and FPGA designs, which occupy a significant role in embedded systems. And we can open a detailed explanation about that in the following sections.

3.2 ASIC design

The complexity of silicon relates to the impact of process scaling and the introduction of new materials or architectures. Many previously ignored phenomena now have a substantial effect on design accuracy [2]:

• Non-ideal device graduation and supply voltage threshold (leakage, power management, circuit/device innovation, the current supplied)

• High-frequency devices coupled and bonded together (noise/interference, signal integrity analysis and management, substrate mating, delay variation due to interconnection)

• Lack of manufacturing stability (statistical process modelling, efficiency, power leakage)

• Degradation of reliability (drilling of insulators, heat dissipation, general tolerance fault)

• Process variability (library characterization, analogue and digital platforms, tolerance for design errors, design reuse, reliability, predictable implementations).

The complexity of a system on chip depends on the exponential increase (according to Moore's law) in the number of transistors per unit area of silicon, stimulated by increased consumer demand for more efficient functions, lower cost and shorter TTM (Time-To-Market) design time, to ensure product profitability.

Finally, there are other additional complexities (such as system environment and/or component heterogeneity) in the system-on-chip integration phase. Design specification and validation become extremely difficult, especially in complex operating contexts. Offsets must be made between all aspects of quantity or quality and all aspects of cost:

• Reuse: supports the hierarchical design and heterogeneous integration of SOCs such as modelling, simulation, verification and testing of component blocks.

• Verification and Testing: Specification Capture, Verification Reuse for Heterogeneous SOC, System and Software Level Verification, Analog / Mixed-Signal and New System Verification, Self-Test, Test Reuse.

• Design cycle cost optimization: cost of manufacturing in modeling and analysis, system optimization for multiple purposes, testability, etc.

• Design of on-board software: use of the platforms adopted for the design methodology, software for verification/analysis of operation.

• Industrial design process control: design team size and geographic distribution, data management, design collaboration.

3.3 FPGA design

The FPGA-based application design market is of increasing interest to traditional CAD vendors. Until recently, the design of a system on chip (SOC) was only accessible to large companies, due to the multiple requirements it entailed (complexity and diversity of skills required, high costs of hardware and software development tools, and large volumes needed to justify the cost of designing an ASIC). Today, two events have changed the situation: the advent of the latest generations of FPGAs and the availability of blocks of intellectual property (IP), [3-6] usable in particular on these programmable matrices, put SOC technology within reach of a much larger audience. Thus, this technology, which mainly targeted the fields: of public, medical, telecommunications and automotive, becomes interesting for more straightforward applications and involves smaller volumes. And this is especially since FPGAs are offered at a meager price (0.0001dollar per gate). In addition, the intellectual property provided for these circuits is now very varied and efficient. First, let us mention the wealth of processor cores: from 8 and 16-bit microcontrollers to high-performance 32-bit microprocessors and DSPs, thanks in particular to the VLIW (Very Large Instruction Word) architecture. To implement these SOC applications, designers must have electronic CAD and embedded software development tools. In SMEs, the first systems-on-chip generally replace existing products using several components (microcontroller, peripherals, etc.). To carry out their projects, these companies need a set of IP blocks that work together and a supplier capable of guaranteeing this interoperability, not a generic SOC design methodology [7, 8]. The IP cores and peripherals chosen for these systems are often copies of discrete components associated with software development tools, of high quality and low price, but offered by different firms [9].

3.3.1 Main manufacturers for FPGA

FPGA manufacturers are constantly improving their products through efficiency and power. The manufacturers who design this type of circuit are Actel, Altera, Atmel Cypress, Lattice, Minc, QuicLOGic, Xilinx and others.

But the main manufacturers that hold an important place in the market are: Xilinx and Altera

The following table gives the Breakdown of the FPGA market:

Table 3.1 part of the market for different manufacturers

MANUFACTURERS	PART OF THE MARKET
Xilinx	35,5%
Altera	32,7%
Lattice	16,1%
Actel	6,7%
Lucent Technologie	4,3%
Autres	4,7%

3.3.2 Different Types of FPGA Circuits

FPGAs can be classified according to their programming technologies. Indeed, to overcome the drawbacks of memories and to make a set of complementary technology adaptable according to the specifications, there are three types of reprogrammable FPGA according to the storage technology to meet the different applications.

These three leading FPGA technologies are:

• RAM programming technology

• Programming technology by EEPROM or FLASH.

• anti-fuse programming technology

a- RAM-based technology (Manufacturers are XILINX and ALTERA)

This technology allows for rapid reconfiguration of FPGAs. The connections are sets of controlled transistors. The major disadvantage of this technology is that it requires a lot of space, and it is necessary to save the design of the FPGA in another flash memory.

b- Technology based on EEPROM or FLASH (The manufacturers are LATTICE and ACTEL) [10]

This technology keeps its configuration but a limited number of configurations with a slower design compared to SRAM

c- Technology based on ANTI-FUSE (The manufacturer is ACTEL)

Table 3.2 gives us the different manufacturers in the world that use these programmable element technologies [10].

Table 3.2 Technologies used by different manufacturers

MANUFACTURERS	**TECHNOLOGY USED**
ACTEL	Anti fusible, SRAM
ALTERA	EPROM, EEPROM,SRAM
AMD	EEPROM
ATMEL	SRAM
LATTICE	EPROM,EEPROM
XILINX	SRAM, Anti fusible, EPROM, EEPROM

The connection points are of the ROM type, i.e. the modification of the point is invertible. To understand the connection mechanism without going into the details of semiconductors, the connection point is considered to be the meeting point of two conductive segments or conductive lines. The "anti-fuse" [11] failure comes from the fact that the initial state of the fuse or the insulating layer is present and there is no contact; to establish it, the fuse must be destroyed, which is contradictory to the usual operation of the fuse. A fuse, less generic but smaller and faster components have been developed.

In the implementation of this work, we have considered making the prototype on a Xilinx ZedBoard Zynq-7000 ARM/FPGA SoC Development Board so that we will focus in this chapter only on the Xilinx technology.

3.3.3 Xilinx FPGA Technology

From the beginning, FPGAs, as Xilinx invented them, had a reputation for providing the user with a fast, reliable and straightforward design [12]. However, technological advances have enabled access to programmable logic matrices of several million gates.

This current complexity remains manageable and allows the realization of compelling applications with a good knowledge of the available resources and respect of a design methodology.

Figure 3.1 shows the simplified architecture of a Xilinx FPGA (for the Spartan-IIE, Virtex-E and Virtex-II families) [13]. The main characteristics of these three families are:

• Complexities range from 1500 to over 8 million gates.

• Low consumption.

• Great flexibility of inputs/outputs with impedance adaptation (Virtex-II) and configuration in differential mode (Spartan-IIE, Virtex-E and Virtex-II).

• Memory functions (distributed and Ram blocks).

• Clock management devices (DLL and DCM).

• Wired multipliers (Virtex-II)

And many other possibilities to optimizethe performance and the density of the logical and/or arithmetic functions.

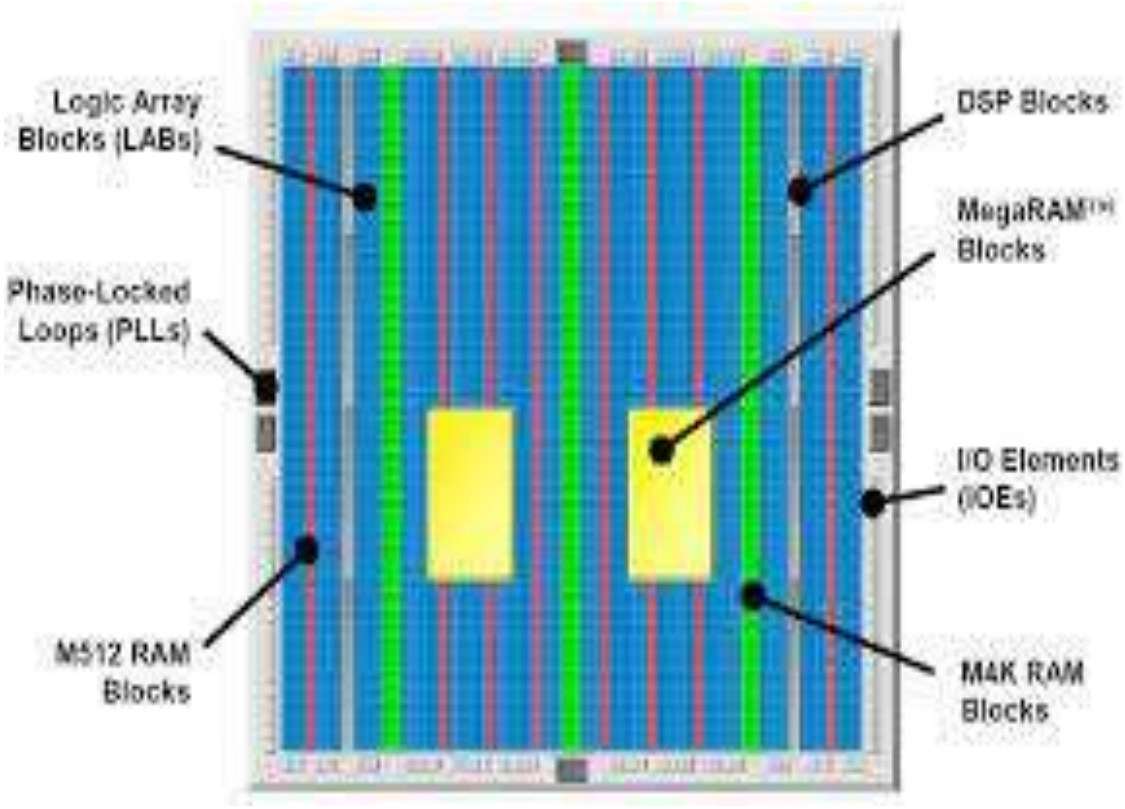

Figure 3.1 Xilinx FPGAs Organization

We see that one of the basic modules is the configurable logic block (or CLB).

It is made up of slices. Figure 3.2 illustrates the simplified architecture of a slice. The combinatorial logic is implemented thanks to each slice's LUTs (Look-Up Table). These LUTs can also be configured as synchronous, single-port or dual-port 16-bit memory elements or as 16-bit shift registers. So there are three ways to configure these LUTs [10]. More precisely, operation in combinatorial mode is obtained by reading the content pointed to by the input signals (Figure 3.3a). In other words, the LUTs are memories whose content is initialized during the FPGA configuration [14]. As a result, they allow the user to have them in "memory element" mode in each of the slices if necessary (Figure 3.3b). Figure 3.3c describes the particular configuration method in the shift register of programmable lengths up to16 bits. Furthermore, additional logic for performing arithmetic functions is available in each slice [15-17]. Thanks to these elements and the appropriate writing style, modules of the accumulator type chargeable in addition/subtraction can be implemented at a rate of 2 bits per slice.

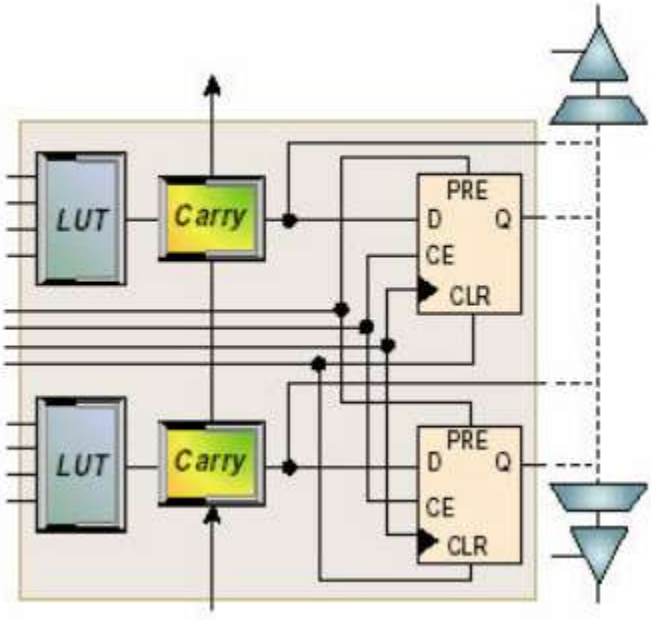

Figure 3.2 Simplified architecture of a "Slice"

The flip-flops in each slice also have essential characteristics for the designer. In particular, they are systematically initialized on power-up (default value '0') and can be used independently of the combinatorial logic available in the same slice. In addition, each flip-flop benefits from control pins such as dedicated clock enable input (Clock Enable) allowing to activate or suspend the operation of each of the flip-flops individually, and this without having to insert any combinational logic on the clock path (synchronous or asynchronous

"set" and "reset" input). The polarity of the clock, "Clock Enable", set and reset signals are programmable for each flip-flop. In other words, these signals can be individually active at the high level or the low level.

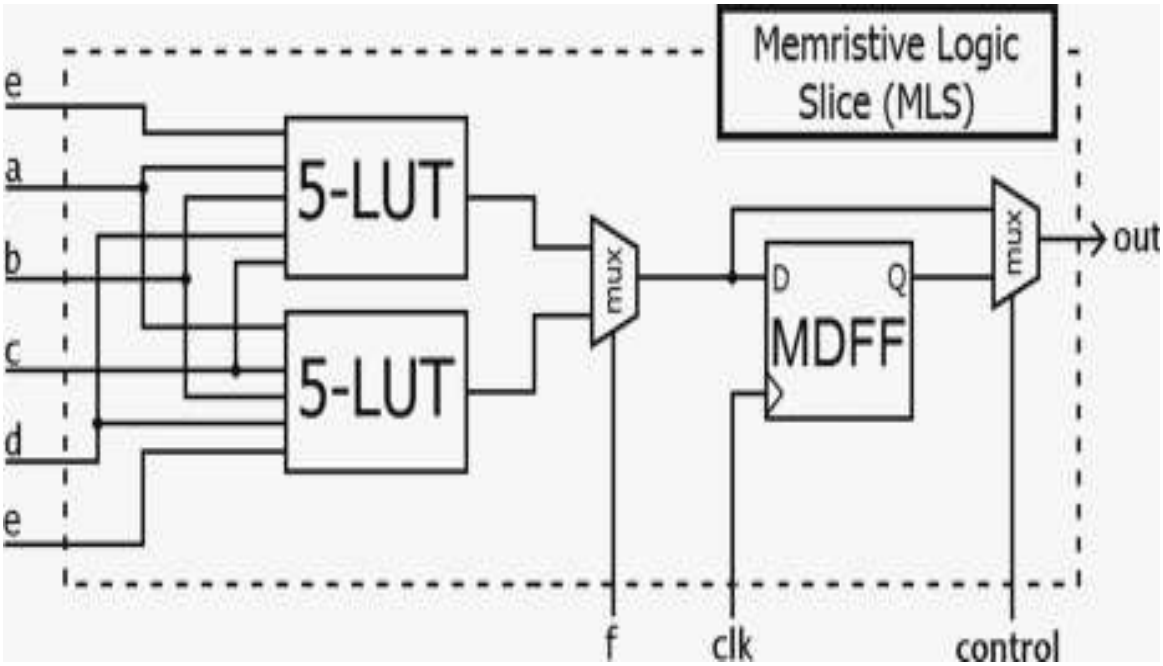

Figure 3.3 LUT configuration modes

2.3.5 FPGA design flow

FPGA manufacturers provide different software tools in their packs, allowing the creation of on-chip embedded systems; among this software, we count ISE (Integrated Software Environment) and EDK (Embedded Development Kit) from Xilinx [12], both offer us the possibility of having a bitstream for programming FPGAs according to the targeted application [18].

The standard design flow consists of several steps:

• Conception and synthesis of the design

• Design implementation and verification

A general view of the design flow is shown in the following figure 3.4

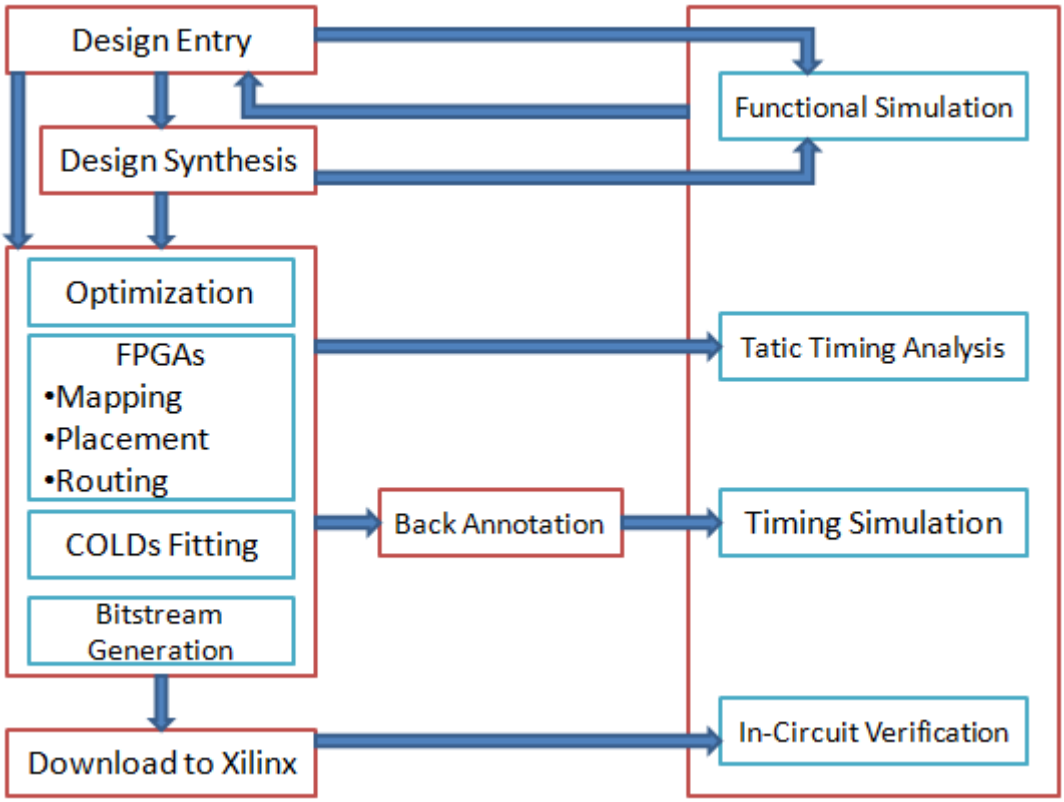

Figure 3.4 Generic design flow

3.4 Xilinx Zynq overview

These days the development of the technological know-how allows brand new corporations to encapsulate distinct components of a device into smaller and smaller devices, all the way down to a single chip, which delivered the System-on-Chip (SoC) notion to the electronics world. I will explain the Zynq-7000 all-programmable SoC by an instance of an SoC. It consists of two complicated processors, programmable common sense (PL), ADC blocks and many different aspects all in one silicon chip.

Before the invention of the Zynq, processors had been coupled with a Field Programmable Gate Array (FPGA), which made the conversation between the Programmable Logic (PL) and Processing System (PS) complicated. The Zynq architecture, in the trendy era of Xilinx's all-programmable System-on-Chip (SoC) families, combines a dual-core ARM Cortex-A9 with a regular (FPGA). Furthermore, the interface between the prime factors inside the Zynq

structure is based totally on the Advanced eXtensible Interface (AXI) standard, which presents excessive bandwidth and low latency connections.

Before enforcing the ARM processor internal the Zynq device, customers have used a softcore processor such as Xilinx's Microblaze. The essential benefit of using Microblaze was, and remains, the flexibility of the processor cases inside a design. Conversely, including a formidable processor in Zynq supplies sizeable overall performance improvements. Also, by simplifying the gadget to a single chip, the gadget's usual price and bodily dimension are reduced.

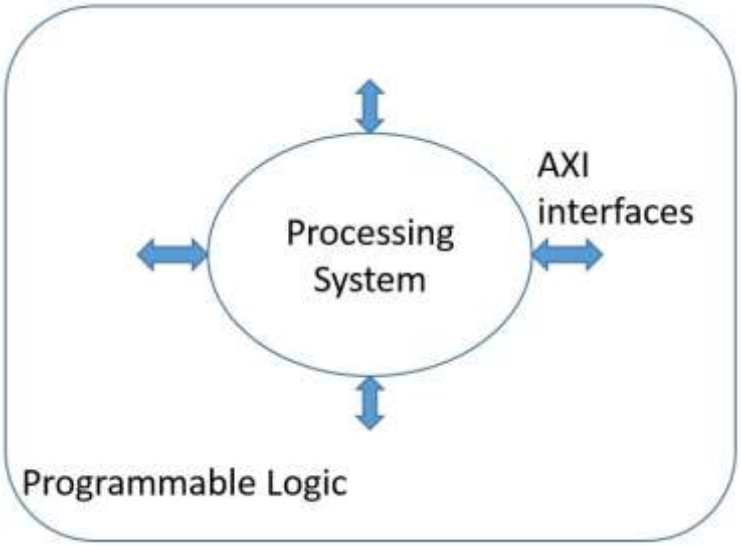

Figure 3.5 Zynq overall views

3.4.1 Zynq Design Flow

The sketch waft for the Zynq structure has some steps in frequent with an everyday FPGA [18, 19]. The first stage is to outline the specs and necessities of the system. Next, at some stage in the gadget format stage, the unique duties (functions) are assigned to implementation in both PL and PS, referred to as undertaking partitioning. This stage is necessary due to the fact the overall performance of the average gadget will rely on tasks/functions being assigned for implementation in gorgeous technology: hardware or software.

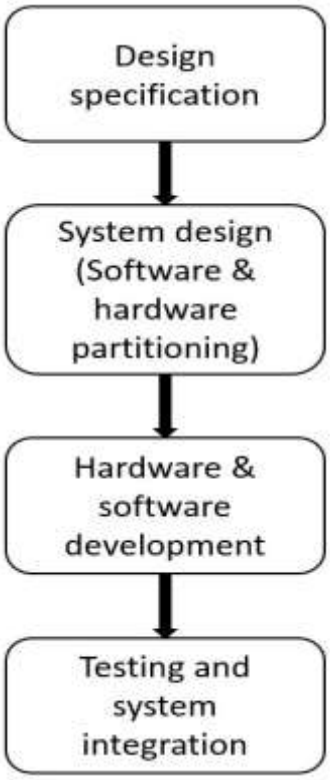

Figure 3.6 Zynq Design Flow Steps

Next, the hardware and software program improvement and checking out must be done. Regarding the PL, the project is to discover the required functional blocks to attain the graph traits, gather them as IPs, and make excellent connections between them. Likewise, the software program endeavor is to improve code to run on the PS. Consequently, device integration and checking out are required to wrap up the design. Figure 3.6 suggests the Zynq SoC graph flow.Inside the Zynq The PS and PL components of the Zynq are defined in this area [13, 20].

3.4.2 Application Processing Unit (APU)

The APU includes two ARM cortex-A9 processor gadgets, every of which usually consists of a NEON unit, floating-point unit (FPU) [21], reminiscence administration unit (MMU) and L1 caches. In addition, the APU additionally consists of snoop manage and L2 caches. Figure 3, suggests the shape of the APU.

- Level 1 cache: Each processor has its very own guidance and information caches for storing the guidelines and data.

- MMU: It is responsible for translating the digital reminiscence addresses to the physical reminiscence addresses.

- Snoop Control Unit (SCU): The interfacing venture amongst processors, L1 and L2 caches is one of the SCU's predominant duties.

- L2 cache: It is shared between the two processors, allowing them to enter the most recent replacement of a variable.

- NEON: The Single Instruction Multiple Data (SIMD) is furnished via this unit which brings necessary acceleration of DSP and media algorithms to the predominant ARM processor.

-FPU: This unit presents the acceleration for the floating-point operations.

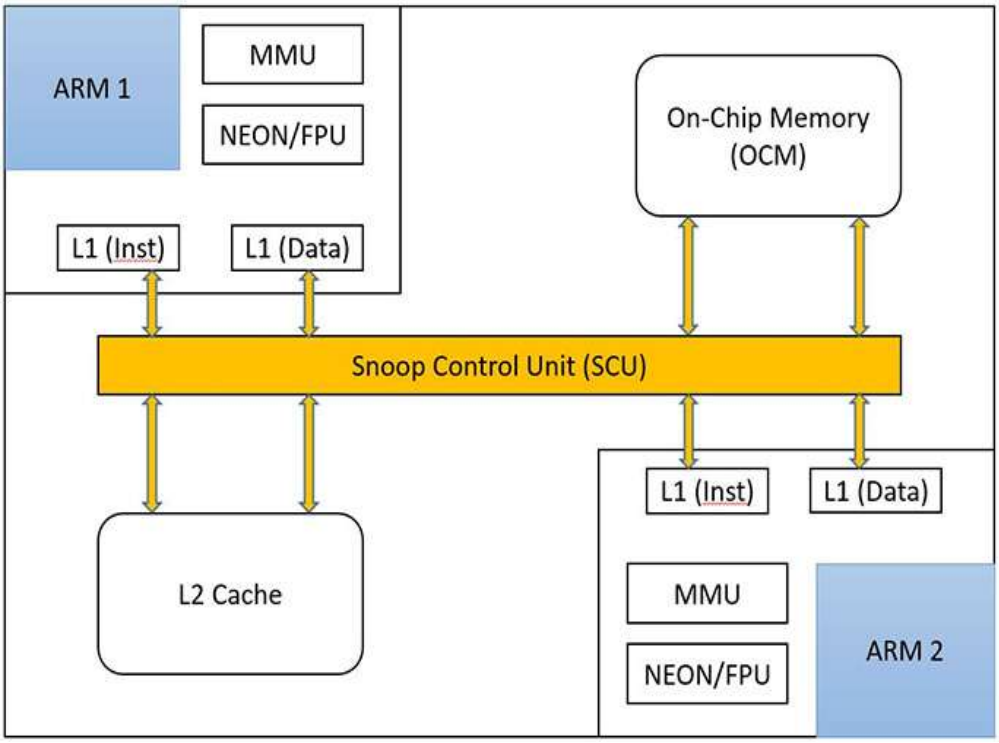

Figure 3.7 Application Processing Unit Structure

3.4.3 Programmable Logic Structure

Like different FPGAs, the programmable common-sense element of the Zynq SoC consists of configurable good judgment blocks (CLBs) that incorporate two slices. Each slice carries 4 look-up tables (LUTs), eight Flip-flops (FFs), and an accompanying swap matrix. Moreover, there are Block RAMs and DSP slices as nicely [8, 21]. Figure 3.8, indicates the shape of the PL.

- Flip-flop (FF): This sequential thing is used to implement a 1-bit register with reset functionality.

- Switch Matrix: It affords the connections amongst the distinctive components inside and between the CLBs, as nicely as different parts of the PL.

- Slice: Each slice consists of assets to implement the combinatorial and sequential circuits [22].

- Look-up Table (LUT): To put in force a common sense characteristic of up to six inputs, RAM, ROM or shift registers, the LUTs are used.

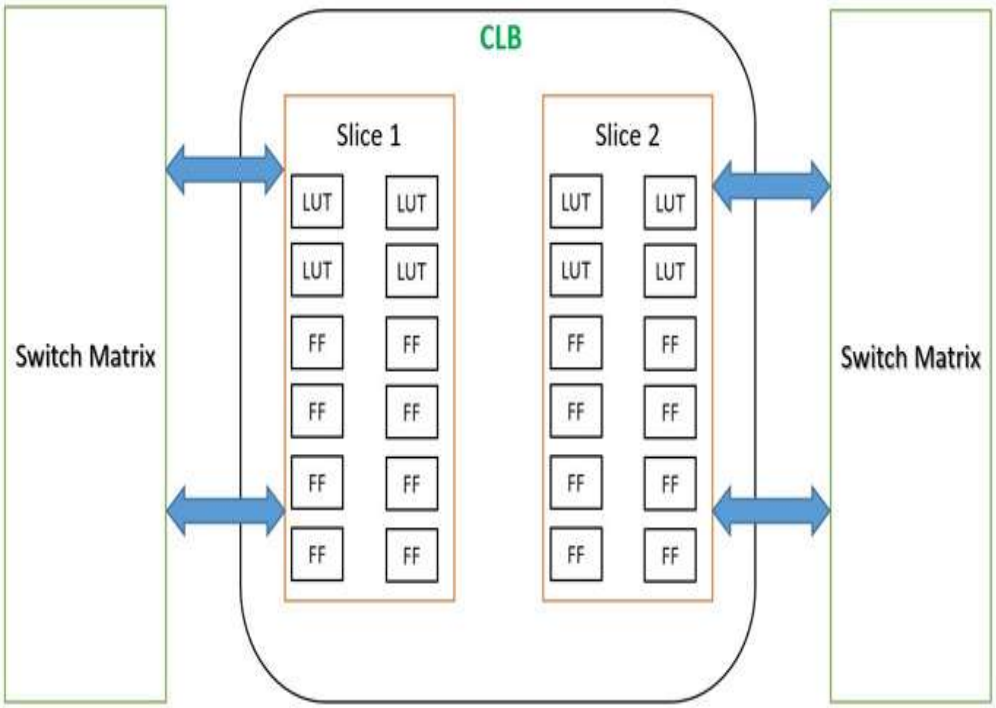

Figure 3.8 Structure of the PL

3.5 Design and Synthesis

A design can be created using a schematic editor or a word processing tool. The procedure begins with a concept expressed by a diagram or a functional description. A netlist is created, synthesized, and then translated from the unique design into an NGO (Native Generic Object) file. This file is then used via a software program known as NGDBuild, which will then produce an NGD file (Native Generic Database) [23].

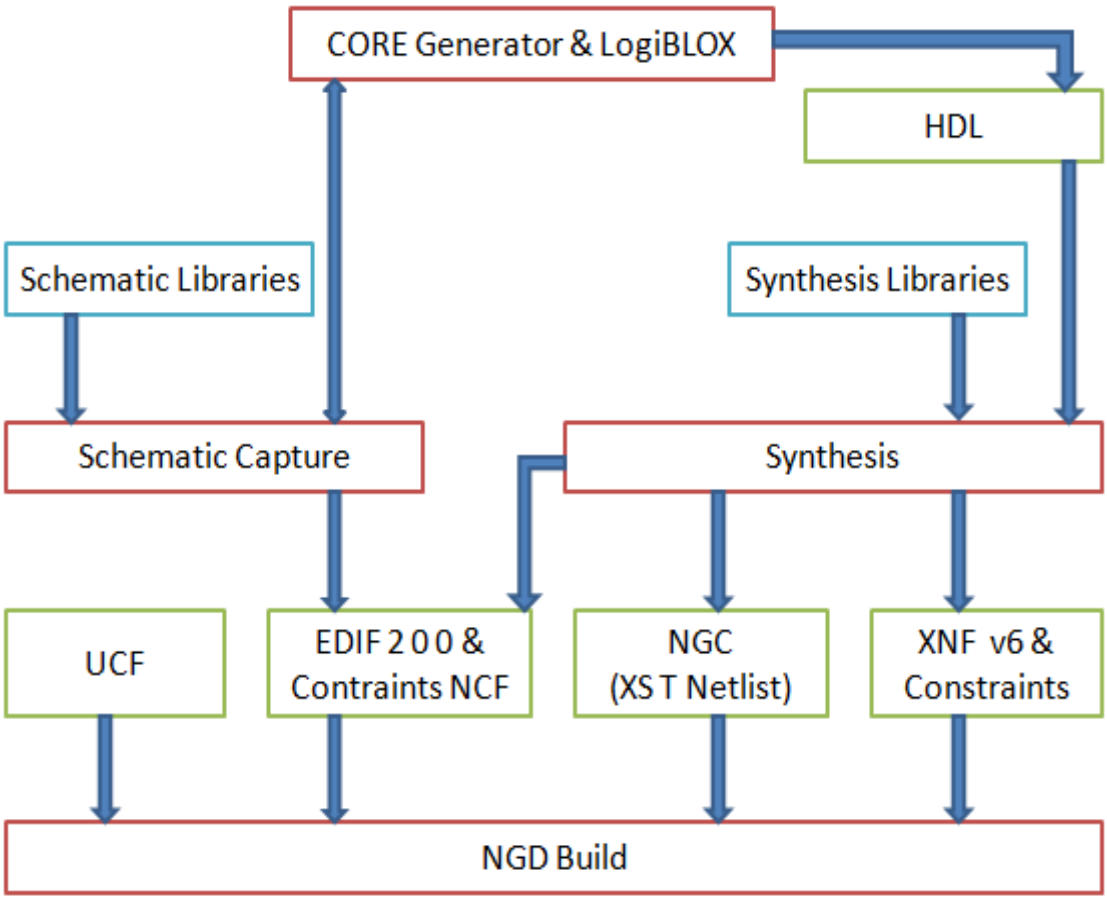

Figure 3.9 Xilinx Synthesis flow

3.6 Hierarchical Design

A design hierarchy is essential in both design modes [24]: Schematic and HDL. And this is for several reasons:

• To have a well-structured design that is easy to debug.

• Combination of several design types (Schematics, VHDL, Verilog, etc.)
• Incremental design consists of individually designing, implementing and verifying parts of the system.
• reduces optimization time and facilitates competing designs by dividing the system into parts that several people will develop simultaneously (like modular design).

3.6.1 Schematics

Schematic tools produce graphical interfaces to describe the design. These tools can be used to connect symbols representing instances of components used in the design. The design can be built using individual ports or functional blocks using library elements.

3.6.2 Elements of Libraries

Primitives and macros are the fundamental constituents of component libraries. Xilinx libraries provide high-level primitives and macros.
A primitive is an elementary part of the circuit (logic gates, Flip-Flops, etc.). Each primitive has characteristic properties (library name, symbol and description). For example, amacro contains several library elements, which can be primitives or macros.
Two types of macros are available for use with Xilinx FPGAs:

• Soft macros whose functionalities are predefined but which are flexible from the point of view of mapping, placement and routing.
• RPMs (Relationally Placed Macros) have fixed mapping and relative placement.

Macros are not available for synthesis because synthesis tools have their module builders and do not require RPMs.

3.7 Core Generation Tool

The Xilinx CORE Generator diagram device affords parameterizable cores that are optimized for Xilinx FPGAs. The library consists of factors that differ from accessible registers to very complicated purposes (DSP filters and multiplexers).

3.8 HDL and Synthesis

A Hardware Description Language (HDL) offers the possibility of multilevel description in which elementary gates and netlists can be used with a functional definition. This level variation makes it possible to describe the system's architecture at a higher level of abstraction, then in an incremental way to refine the design implementation up to the level of the doors.
The HDL description offers the following advantages: the functionality of the design can be verified immediately, which allows architectural decisions to be evaluated, an HDL description is easier to read and understand than a netlist or a schematic illustration, and it constitutes design documentation and its technology-independent functionality, not to mention that an HDL description makes it easier to handle large designs than a schematic description.

After creating the design in HDL, it must be synthesized. During synthesis, the behavioral information in the HDL file is translated into a structural netlist, and the design is optimized for Xilinx components. The synthesis tool used by ISE is XST or Xilinx
Synthesis Tool.

3.9 Functional simulation

After its design and description, the functional simulation tests the logic of the design to detect and correct any malfunction due to poor design or erroneous description. The software used for functional simulation is ModelSim.

3.10 Constraints

Constraints are used to force the system to work within a particular time or surface limitations. Restrictions can be introduced manually or using the constraints editor, floor planner or FPGA editor (tools accompanying ISE).
Timing Analyzer or TRACE can be used to evaluate the circuit after implementation under these constraints.

3.10.1 Mapping Constraints

To specify the mapping of a logical block in the CLBs, the FMAP or HMAP constraints (for certain families) can be used. However, excessive use of such constraints can make routing difficult or even impossible.

3.10.2 Placement Constraints

The placement of a block can be forced to a specific given position. The location can be specified in the schematic description, synthesis tool, or a UCF file (User Constraints File). The wrong placement of a block can prevent the design from being placed and routed completely. Typically, only the input/output blocks require placement constraints so that they are in the correct positions concerning the pins.

3.10.3 Time constraints

This is to specify timing constraints to limit the propagation time of signals along processing paths. The PAR Place and Route tool use these constraints to achieve optimal performance during the Place and Route operation.

3.10.4 Translation to Net List

The format required by Xilinx development tools to complete the design flow is NGD (Native Generic Database). Two mechanisms are available for translating from other forms to NGD. For example, EDIF2NGD translates a fileEDIF (Electronic Data Interchange Format) to NGD, and the NGDBuild program converts several formats (XNF, or EDIF) to NGD. Note that this last tool uses the first to translate EDIF files.

3.10.5 Implementation

The design implementation begins with the mapping, which results in the association of the logical elements with the physical aspects of a given component. It ends when the physical design is fully routed and translated into a series of bits loadable in the element.

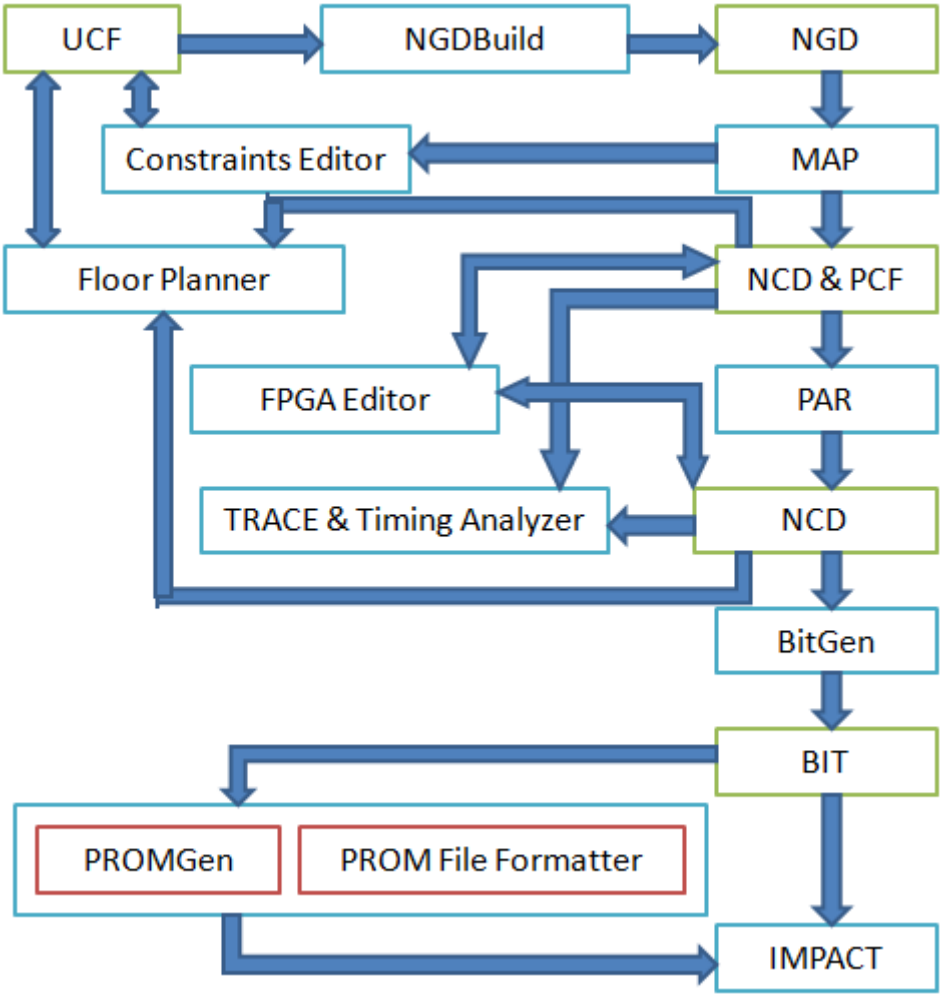

Figure 3.10 Implementation Flow

3.10.6 Mapping

The MAP tool arranges the logical elements of a design in a Xilinx FPGA and associates them with physical elements. The MAP tool takes as input an NGD file that contains a logical description of the design in terms of hierarchical components used in the design and low-level Xilinx primitives and any number of hard-placed and routed macros (NMC) files.), Each

contains the definition of a physical macro. MAP then associates components (logical cells, input/output cells, etc.) with the different logical parts of the design. The MAP output is a Native Circuit Description (NCD) extension circuit description file. This file is a physical representation of the design using the building blocks of the target FPGA. The NCD file can be placed and routed.

3.10.7 Placement and Routing

The PAR (Place And Route) tool takes as input a physical description of the design (an NCD file), places it and routes it to give another NCD file, usable by BitGen so that it is transformed into data of configuration. The output NCD file can also be used as a guide file to redo the routing placement after making minor changes to the design. The FPGA editor tool allows you to place and route critical components before launching the automatic placer/router and also allows you to modify the placement and routing manually.

3.10.8 Bit stream generation

The Bit Gen tool produces a series of bits for configuring a Xilinx FPGA. BitGen takes a fully placed and routed NCD file to generate the series of configuration bits as a .bit extension file. The BIT file contains all the information contained in the NCD file (the internal logic and the interconnections between the elements of the FPGA), and characteristic information of the target component from other files associated with the target component. After generating the BIT file, it can be loaded into the FPGA using the iMPACT tool. A PROM file can also be created from the BIT file to load it into a PROM, to be used later by the FPGA.

3.10.9 Verification

Design verification is a process of testing design functionality and performance. Xilinx offers several methods for this purpose:

- Functional and temporal simulation
- A static temporal analysis
- Verification on the circuit

The design verification procedure is usually done as shown in the figure:

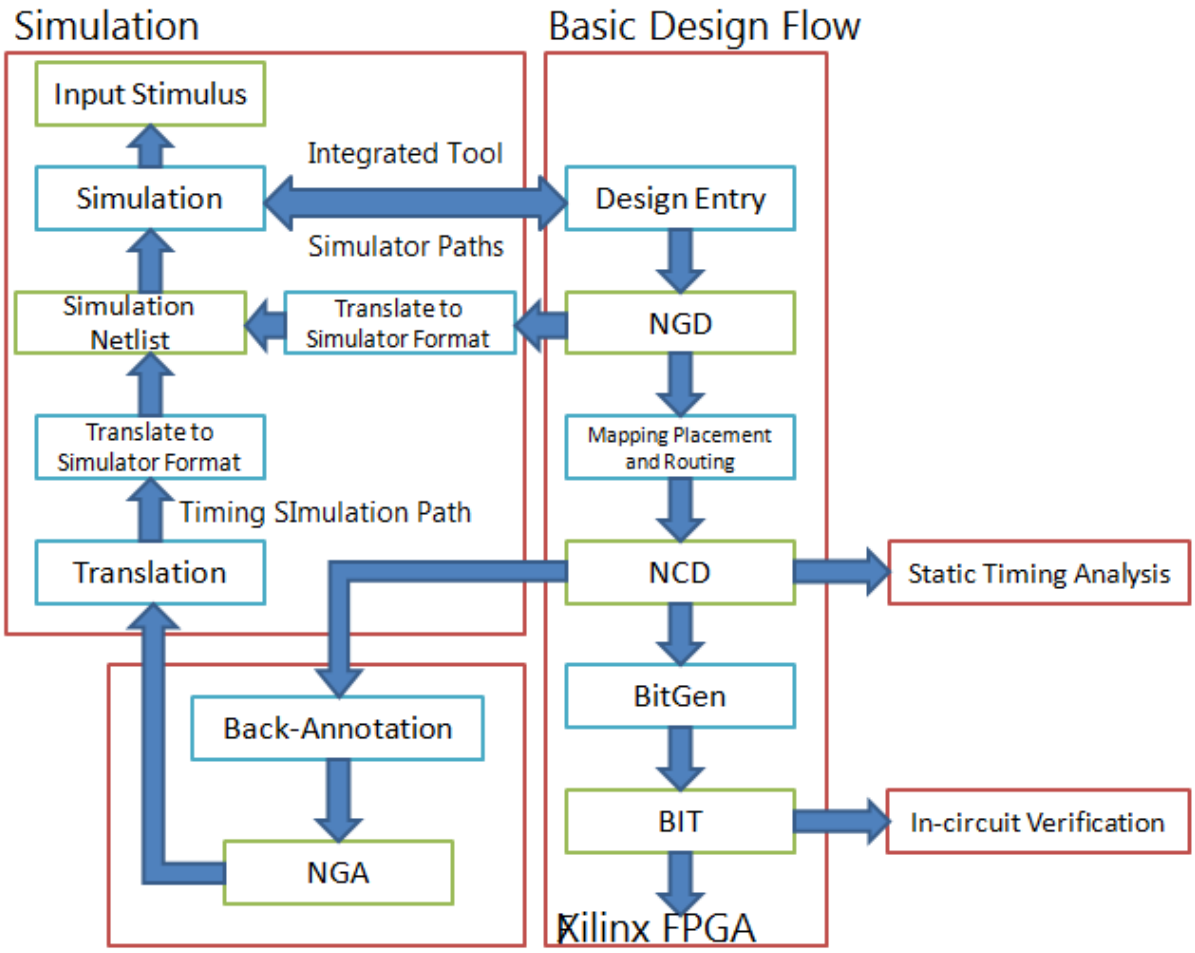

Figure 3.11 verification steps

To verify the design, a functional or temporal simulation can be run.A Back-Annotation process must take place before the temporal simulation. Before the temporal simulation phase, the physical description of the design must be translated into a logical design understandable by the simulator. This task is called the Back-Annotation process in English.

A tool called NGDAnno is responsible for creating a database for use by the netlist creator tool, which translates this information into a netlist format understandable by the simulator. The following figure illustrates the Back-Annotation process.

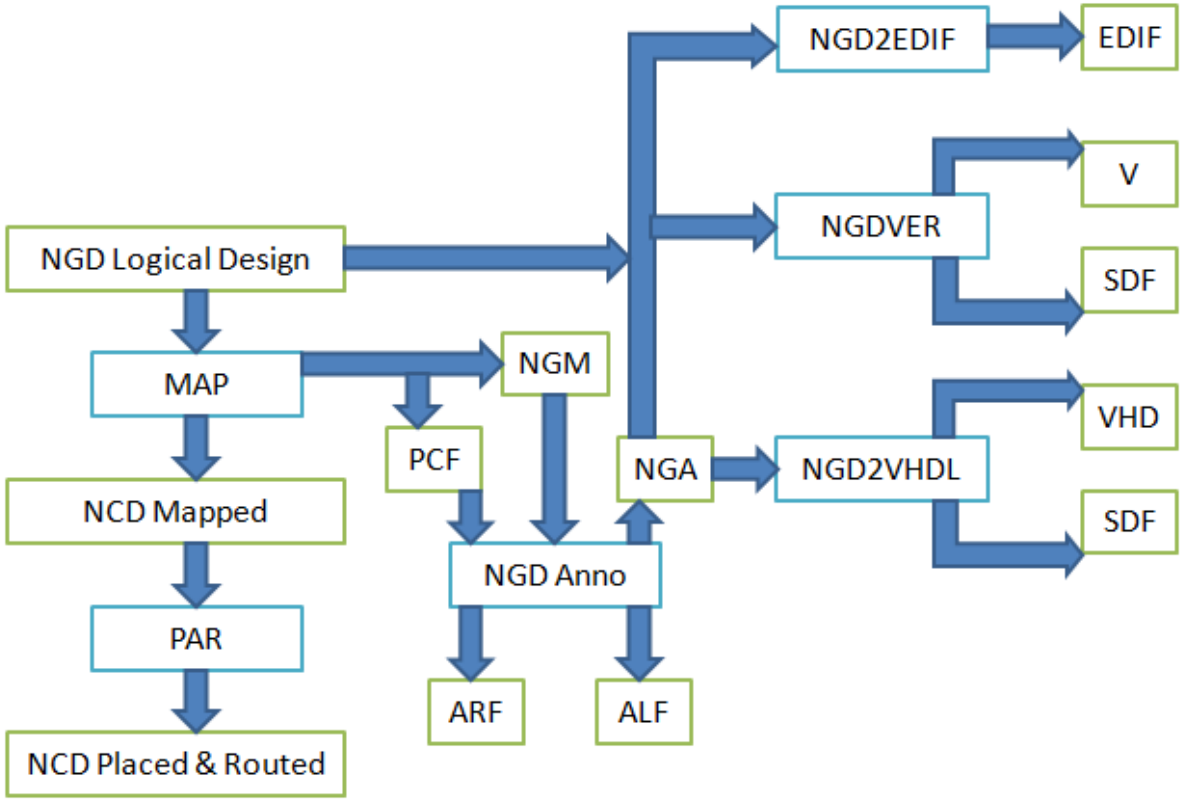

Figure 3.12Back-Annotation Processes

NGDA nno is a tool that translates the physical characteristics (delays, signal propagation times, response times, etc.) found in an NCD circuit description file into a logical description file of the NGD design (taking into account all the physical characteristics of the circuit). The input NCD file can be a fully or partially placed and routed design or a non-placed or routed design (NCD output from the MAP tool).

An NGM file also created by MAP is an optional entry for NGDAnno, which merges the mapping information contained in this last file with the placement, routing and timing information from the NCD file used. On output, this tool generates an NGA (Native Generic Annotation) file, which is an NGD file reconstructed from an NCD. This file will be input to the appropriate netlist generator tool, which will convert the design from binary NGA format to ASCII netlist format. The netlist writers (NGD2EDIF, NGD2VER or NGD2VHDL) take the output of the NGDAnno tool and create a simulation netlist in the specified format. An NGD file or NGA can be an entry for a netlist writer. NGD2EDIF translates an NGD or NGA file into netlist in EDIF format (EDN file). NGD2VER translates an NGD or NGA file into a netlist in Verilog format (V file). This tool also generates another SDF file (Standard Delay

Format) which contains time information that is usable only with the Verilog file created by the same device, from the same NGD or NGA file. NGD2VHDL translates an NGD or NGA file into a VHDL netlist (VHD file). If the input file is in NGA format, this tool generates a specific SDF file for this VHD file. And talking about VHDL as mentioned in section 3.12in detail.

3.10.10 Schematic-based Simulation

Design simulation is the act of testing the design using software models. Testing the design and its performance under the worst conditions is more efficient. This model allows viewing the internal nodes to examine the circuit's behavior and use the results to change the schematic description of the design. The simulation is done using third-party tools linked to the Xilinx development system. The software models offered for the simulation tools are designed to present the detailed characteristics of the design.

3.10.11 Functional Simulation

The functional or behavioural simulation determines if the design logic is correct before the implementation phase. This type of simulation can take place early in the system design process. And since timing information is unavailable now, the simulator tests the logic using elementary delays as units. The simulator (ModelSim) is integrated into the Xilinx development environment: switching between the design tools (HDL or schematic editors) and the simulator is done automatically without the need for intermediate use of translation tools.

3.10.12 Temporal Simulation

Temporal simulation examines the execution time of the design under the worst conditions. This process can take place after design mapping, placement, and routing. At this time, all design deadlines are well known. Temporal simulation is essential because it can verify temporal relationships and determine critical design paths under worst-case conditions. Before the temporal simulation, it is necessary to go through the Back-Annotation process already mentioned.

3.10.12 HDLbased Simulation

Xilinx offers the possibility to perform functional and temporal simulations of designs expressed in HDL at several levels see Figure 3.13

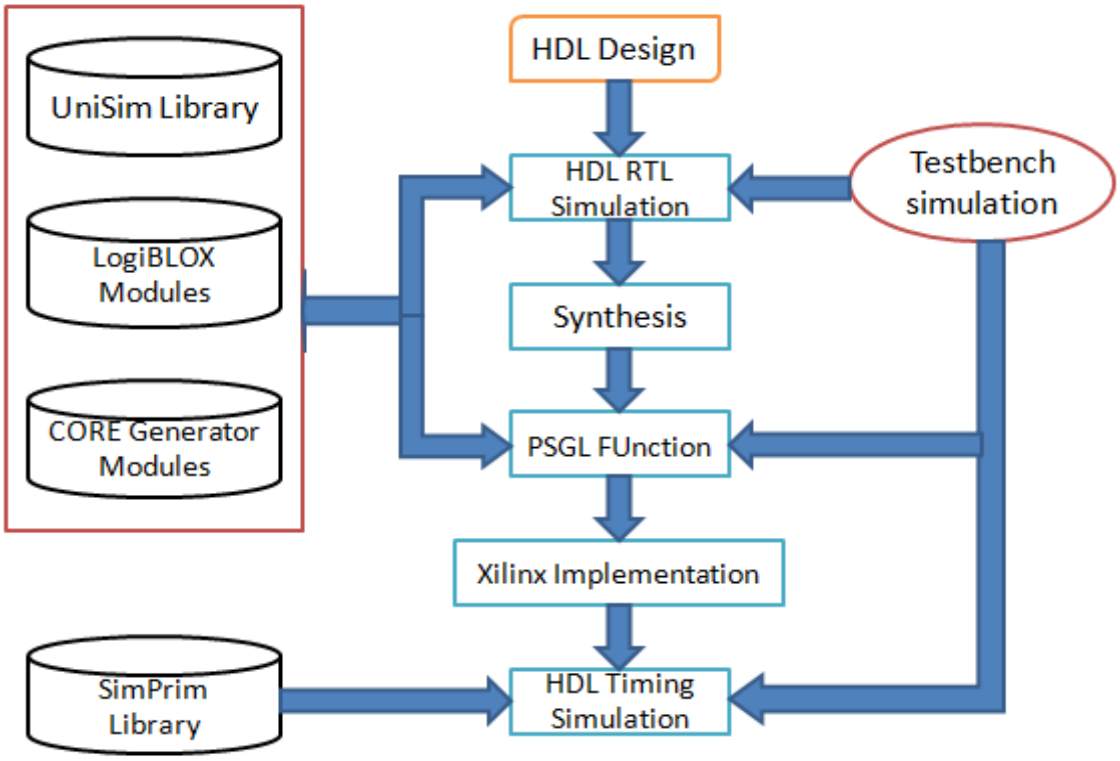

Figure 3.13simulation procedure of a modelsim SoC

Simulation at the RTL level (Register Transfer Level), which can contain models LogiCORE and instances of components from the UniSim library, at the post-synthesis level (functional simulation), at the post-implementation level (temporal simulation after the Back-Annotation process).

3.10.13 Static Time Analysis

Static temporal analysis is favored in the case of rapid verification of a design after placement and routing. It allows for determining the deadlines of the design paths. The two primary purposes of temporal analysis are temporal verification (verifying that the design obeys temporal constraints) and reporting (describing temporal behavior in a technical way that can

be used as documentation to evaluate the design). The TRACE tool (Timing Reporter And Circuit Evaluator) is responsible for this analysis.

3.10.14 Circuit Check

Verification of design behavior in the target application is considered a final test. The validation of the FPGA design on the test circuit is a circuit under typical operating conditions. This type of testing is simple because Xilinx components are reprogrammable (several iterations of the design can be tried).

Before growing the remaining BIT file, it is beneficial to use the DRC alternative in the BitGen device to consider the NCD file and look for problems that may also stop the graph from working correctly on the goal component.

3.11 Xilinx System Generator

System Generator is a DSP design tool from Xilinx that enables the use of the MathWorks model-based Simulink design environment for FPGA design [13]. The design tools facilitate the design processes by obscuring the technical knowledge necessary for FPGA a Register Transfer Level (RTL) design.

Instead, a plan has modeled the intuitive visible surroundings inside Simulink that uses numerous precise block units to speed up the development. Additionally, System Generator can function in the FPGA implementation steps: synthesis, mapping, and region and route to generate the FPGA executable file. Figure 3.14 indicates the diagram waft

the use of the Xilinx System Generator.

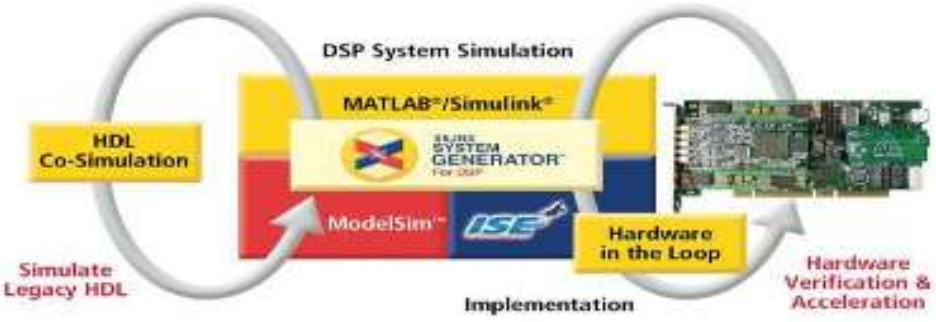

Figure 3.14: Design flow for Xilinx System Generator

This design flow can be adopted to develop and test an ECG signal filtering system and may also need programming like VHDL.

3.12 VHSIC Hardware Description Language (VHDL)

The VHSIC program (Very High Speed Integrated Circuits), promoted by the United States Department of Defense in the 1970s and 1980s, gave birth to a language: VHSIC-HDL, known as VHDL. [27]

The VHDL description language then became an IEEE standard in 1987. Revised in 1993 to remove some ambiguities and improve the portability of the language, this standard quickly became a standard for logical function description tools.
To date, we use the VHDL language for:

• Design ASICs,
• Program programmable components of the PLD, CPLD and FPGA types,
• Design digital simulation models or test benches as mentioned in [28].

The purpose of a hardware description language such as VHDL is to facilitate the development of a digital circuit by providing a rigorous method of describing the operation and architecture of the desired circuit.

The next step involves synthesizing this hardware description to obtain a component performing the desired functions, using concrete logic elements (logic gates, flip-flops or registers). Depending on the technology used, these will be implemented, either directly in transistors (in the case of an ASIC) or based on the programmable elements of FPGAs.

Since VHDL has a dual function (simulation and synthesis), only part of VHDL can be synthesized, the other existing only to facilitate simulation (writing of behavioural models and test benches) [29].

2.13 Conclusion

At the hardware level, the realization of a system on a chip today is more accessible thanks to high complexity FPGAs combined with IP blocks. On the other hand, developing the software embedded in these SOCs, often comprising several configurable cores, requires an upgrade of the compilation, assembly and debugging tools.

Currently, most CAD software vendors focus on the high-end market, offering expensive tools to a limited number of developers. In contrast, runaway software tool vendors focus primarily on the primary market.

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Chapter IV: ECG de-noising and FPGA implementation

4.1 Introduction

Electrocardiogram (ECG) is a critical biomedical signal, and the processing of the ECG signal is not only recommended but vital [1][2]. However, that ECG signal is corrupted by different noises inside and outside its frequency band (0.01-128 Hz). Hence, extracting useful information from the distorted signal is difficult, because the corruption signal is created due to biological sources such as the human body and ecological sources such as data collection devices [3]. For example, instrumentation noise refers to the noise that originated in the data collection device, the electronic noise, which is a specific kind of instrumentation noise. This kind of noise is referred to as flicker noise which overlaps in the frequency domain with EMG (electromyography) noise. Therefore, filtering the EMG noise will reduce these flickers [4]. In addition, other noise sources affect the ECG signal, such as channel noise, electrode contact noise, motion artefacts, etc.

This thesis addresses prominent noises: EMG noise, power line interference noise, and baseline drift noise [5].

The first type is EMG noise which emerges because of the contraction of muscles other than cardiac muscles [6] and is assumed to be transient bursts of zero mean bands limited Gaussian noise [7]. It is overlapped with the ECG signal at the moment of heart electrical activity recording, including the amplitude of this kind of noise; it is random and could be reasonably approximated by a Gaussian function in the range of 0 to 100mV. Hence the ECG signal's amplitude ranges from 0.1 to 5 mV. Therefore, EMG noise and ECG signals participate in the frequency spectrum with significant parts of energy [4]. Thus, EMG noise operates in the high-frequency range, i.e. (>100 Hz), so it can be removed by using a low pass filter (LPF).

The second noise is power line interference (PLI), which mostly happens due to the unsuitable grounding of the ECG device. This noise affects the signal's quality and detailed features, which can be critical for signal processing because these features are rich sources of information. In addition, it operates in medium frequency, i.e. (50Hz/60Hz). This noise can be suppressed by the band stop filter (BSF).

The third noise is the Baseline wanders (BLW); body actions, respiration, sweat, and improper electrode connections are the primary sources of this noise. According to Nyquist’s

rule, its frequency range is usually between (0.1Hz-0.5Hz); its low frequency can be eliminated using a high pass filter (HPF). Finally, de-noising ECG signal is a chain of steps taken to decontaminate the original ECG signal from noise.

As ECG and some noises share the same frequency, the best de-noising technique is the one that provides the best trade-off in terms of minimal wastage of information and an interesting level of noise elimination [8].

Within the scope of our knowledge from the proposed method experiments, it has been noticed that the process for noise disposal depends on several factors that directly affect the filter results and the quality of the accompanying signals. These issues can be explained in the following points [1], [2].

How to select the position of each filter in the combination of cascaded filters? I.e.which one among these filters should be the first, intermediate or the last?

Then, how do we determine the cut-off frequency bands in the appropriate order for each filter?

And what are the sorts of windows used for configuring the filter or any other technique for filtering the signals?

Moreover, how to provide the window parameters?

So, the ECG signal is contaminated by multi-levels of noises, a cascaded filter can remove different noises depending on desired frequencies, which involves many steps such as shown in Figure 4.1.Therefore, an FIR filter can be designed with varying methods of windowing. But there is a critical remark to the point which concerns the fact that the arrangement of the windows with filters position has not been covered in the other mentioned literature algorithms, this problem that we checked and analyzed in this study through the few papers of this thesis manuscript.

However, the following sections will show the detail of the ideas of ECG signal de-noising using the windowing selection based on the cascaded FIR filter [1] with revealing and evaluating the Influence of filters position in the cascaded FIR filter too [2], in which that's tested on the ECG signal de-noising with three levels of courant noises. The use of this issue should not be random due to its impact on the quality of the resulting signal. As a resolution, the filters' arrangement with windows selection in the cascaded filter has been affected by the parameters and the combinations of the filtration systems i.e. the arrangement of the windows with the filters are played a vital role in significantly improving the cascaded filter performance in the task of signals filtration.

These latter ideas constitute the originality of this contribution. So, this study aimed to characterize each type of window (adjustable or fixed window), such as Kaiser and Rectangular windows of various SNR levels (0 to 10 dB) and to assess the effects of the filter position arrangement on different ECG signals. Nevertheless, this contribution provided significant effectiveness and superb potential in the design of the filters. The cascaded FIR filter system had been implemented on FPGA using the basic Xilinx System Generator (XSG). To evaluate the proposed algorithms' performance and effectiveness, we have used a (PTB) diagnostic database.

4.2 Methodology of ECG signal De-noising using FIR Filter

Many other methods are used for designing FIR filters such as equiripple, least square, and maximally flat, instead of the windowing method, regarding the ECG de-noising problem [9].In addition, many studies have been made to prepare the combination of various digital filters, i.e. high pass filter, band-stop filter and low pass filter, to remove the noises BLW, PLI and EMG, respectively, from ECG signal.

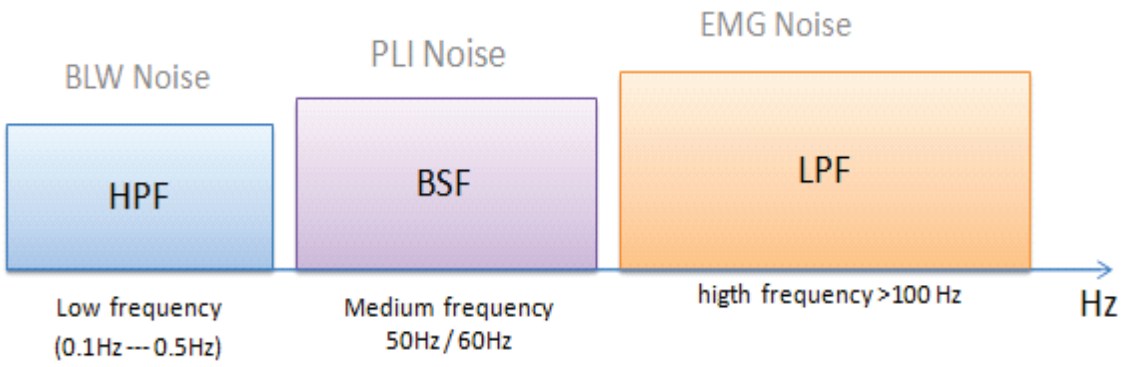

Figure 4.1 Filter types corresponding to major noises' frequency

Figure 4.1 shows different noises compatible with various appropriate frequency bands based on digital filter types, respectively. Moreover, all the preview works have adopted the windowing method to design the cascaded FIR filter.

4.2.1 Digital FIR Filter

Finite Impulse Response (FIR) filters are the only essential digital signal processing system parts. On the other hand, the Distributed Arithmetic (DA) algorithm characteristics are preferred due to considerably scaled back hardware size utilization which ends up in high-speed execution [10].

FIR filter generally has a linear-phase response. The impulse response of a linear-phase FIR filter has even or odd symmetry which can be used to exploit and reduce the number of multipliers [11].
Finite impulse response filters are also recognized as non-recursive digital filters; these filters are often used in digital signal processing owing to their flexibility, i.e. can be adapted according to the need and more efficiently than analogue filters [12].

However, there are three main methods for FIR filter design, namely:

- Optimal Filter Design Method.
- The frequency sampling technique.
- The windowing method.

Different windowing methods can design the FIR filter. There are two window kinds, namely: fixed and adjustable windows.
A digital FIR filter of M order has the transfer function that can be described by:

$$Y(m) = \sum_{k=0}^{M} b_k \, x(m-k) \qquad (4.1)$$

The response of such a filter to an impulse is composed of a finite sequence of *M+ 1 sample*, where *M* is the filter order. Hence, the output *Y(m)* of an FIR filter is a function only of the input signal *X(m),* and *bk* are the filter coefficients [13].
For digital FIR filters, a (compiler 5.0 block set) is used, such as digital filters in our simulation experiments; the filters are applied with a fixed order, the sampling frequency of (360 Hz >= 2*(original ECG signal)) and cut-off frequency selected according to the undesired noise frequency. So, these material equipment and Simulation methods are

combined to achieve our main aims and fill in the results of the experiments noted in the following tables in the following sections.

4.2.2 Cascaded Filter Technology

The cascade filter works like the tool we use to filter water with many impurities just as it allows us to remove the noise associated with the signal. It has practical advantages, which is to process multi-levels and frequency bands simultaneously, and it can also be configured from different types of well-known filters mentioned in Chapter Two.

4.2.3. FDA Tools and Window Function

The Filter Design and Analysis (FDA) tool is essential for creating filter transactions. The options available depend on the specific filter design method [14]. There are two types of window functions described by an adjustable window and fixed window [11], such as appearing in Table 4.1. On the other hand, the FIR equiripple and FIR window design methods have settable options. For FIR equiripple, the choice is a density factor. For the FIR window, the possibilities are Scale Pass band, window selection, and for the following windows, a settable parameter [14]. The adjustable window has been set up with one or more parameters provided, as shown in Table 4.1

Table 4.1 Adjustable windows parameters

Adjustable window	**Provided parameters**
Chebyshev	Sidelobe attenuation = 102 dB
Gaussian	Alpha _ $\alpha = 2.8$
Kaiser	Beta _ $\beta = 0.5$
Taylor	Nbar = 5 Sidelobe level = -30 dB
Tukey	Alpha _ $\alpha = 0.5$

4.2.4 ECG Database Overview

The records were digitized at 1000 samples per second per channel with 16 bits resolution (14 bits for ECGs, 01 bit for respiration effect and01 bit for line voltage effect) over ±16 mV ranging from (0 to 65535) [15], i.e. 32768 which is the midpoint of resolution that is worth 0 mV.

Therefore, from the raw ECG signal, as mentioned in [15], the effects of BLW and PLI noises originally are associated with it from the Physiobank ATM (PTB diagnosis ECG database), as shown in Figure 4.5.
The ECG samples data file from the PTB database is extracted and considered as the original ECG signal with low and Medium frequency noises. Experimentally, the same samples data was just added to identify the proposed work's performance levels, as shown in Table 4.4 below.

4.2.5 White Gaussian Noise (WGN) and EMG Approximation

As previously mentioned, the records taken from the database in force on this proposal contain two types of noise inherent in the raw ECG signal: the BLW and PLI [15]. If anticipated, non-stationary in the raw ECG signal, the noises that corrupt it, such as EMG and others, are also non-stationary [4]. Hence, this means that EMG noise is overlapped with the ECG signal, and they are exact, and then this noise has the same high-frequency feature as WGN. Advocating, in this paper, the WGN with -27.42 dB is adopted as the muscles contraction effect source, and embedded in the ECG signal, which distorts the information signal and lowers its quality to achieve different SNR levels [16]. This is evident in the raw signal and the mark representing whole noise contamination, as in Figures 4.5- 4.10 below.

4.2.6 SNR and MSE Parameters

ECG Signal de-noising approaches are usually estimated by the signal-to-noise ratio (SNR) and mean square error (MSE) parameters on dB [2]. Furthermore, these parameters can know how close the de-noised signal is to the original signal assessment.

$$SNR = 10\ log_{10}\left[\frac{\sum_{n=1}^{N} x(n)^2}{\sum_{n=1}^{N}(y(n)-x(n))^2}\right] \quad (4.2)$$

$$MSE = \frac{1}{N}\sum_{n=1}^{N}(y(n) - x(n))^2 \quad (4.3)$$

Eqs (1) and (2) are used to calculate SNR and MSE of the filtered signal, respectively, where *x(n)* is the original ECG input signal, *y(n)* is the output de-noised ECG signal of digital filters, and *N* is the sampling points of ECG signals [17]. Hence the better de-noising method should have a higher SNR and a lower MSE.

4.3 ECG Preprocessing and Filtering Methods

A cascaded window based on a digital FIR filter design is presented. Three sets of FIR filters are adopted to remove noises from the ECG (Electrocardiogram) signal. These noises can be classified into three main types: electromyography (EMG), Power Line Interference (PLI) and Baseline Wander (BLW), which themselves occupy three frequency bands: high, medium and low frequency, respectively. This contribution is intended to improve the ECG signal's quality.

The resulting performance is evaluated on the (Physikalisch-Technische Bundesanstalt) (PTB) diagnostic database. Two approaches are considered for this task; the performance of the cascaded FIR filter is tested for multi-level frequency.

The comparisons are based on Signal to Noise Ratio (SNR) improvement and Mean Square Error (MSE) minimization.

4.3.1 ECG De-noising based on the Selection of Cascaded FIR Filter Windows

For decades, private centers in hospitals have collected and stored data from patients' health care, to refer to them in many cases, such as diagnosis of morbidity and post-clinical follow-up of individuals or general statistics, even more, conducting continuous scientific research to develop the field of biomedical, medicine in general, such as chronic disease detection and prevention, drug extraction and organs' surgery. Thus, the ECG database can be obtained in

the hospital ECG monitoring device, or it can be obtained by hand tools available in laboratories such as ECG Simulator Multi-Parameter Patient Monitoring device. But in our study of the ECG signal processing, the Physionet Database from Physiobank Library is used [15], which is freely available online, where could find many previously recorded ECG patterns such as a text header file, binary annotated file and binary data signal file. The recorded signals have been retrieved from Physiobank ATM – export signals as (mat) format to experiment manipulation and implement using MATLAB and SIMULINK environments.

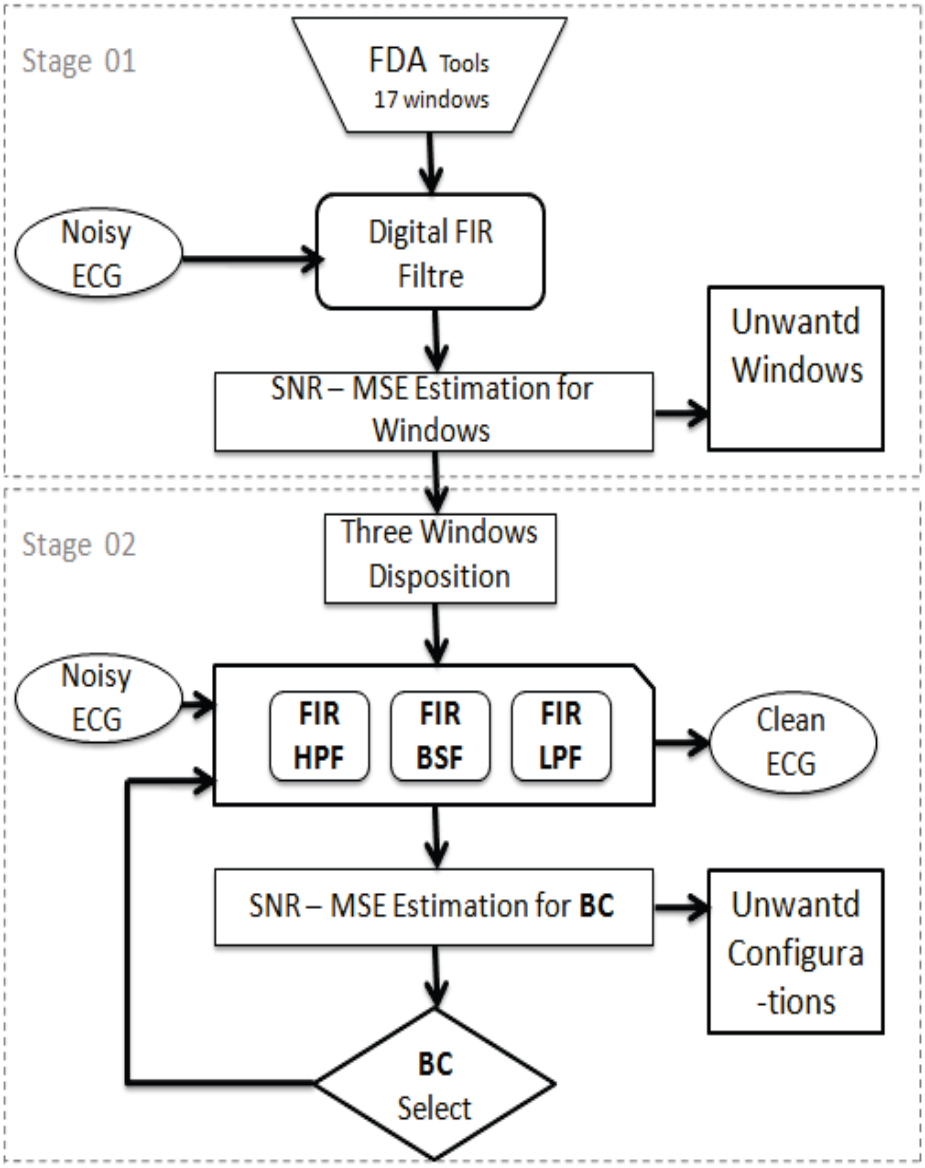

Figure 4.2 Diagram of the proposed method

Figure 4.2 illustrates a detailed work plan that lists the steps identified to reach the desired results. As mentioned above, this proposed method is divided into two parts and may seem separate in appearance, but each portion complements the other. The following steps illustrate the algorithm procedure.

Algorithm Pre-Processing Captured ECG signal
Input: Noisy ECG signal *E* Input.
Output: ECG without noises *E* Output.

Stage 01: Select the Three Windows.

1: Load *E* Input

2: Initialize each filter type separately (HPF, BSF, then LPF), by choosing orders, cut-off frequency and simple frequency in FDA Tools.

3: Filtering *E* Input signal by using all window methods (17 windows) available in FDA Tools.

4: Computing and comparing all 17 results according to SNR and MSE parameters for each filter, and select the desired three windows.

Stage 02: Select the Best Configuration (BC).

1: Load *E* Input.

2: Insert the three windows resulting from the first stage and distribute them on cascaded filters.

3: Filtering ECG signal by using all possible configurations (27 configurations) applied to cascaded FIR filter.

4: For each configuration, measure the SNR and MSE parameters and select the best arrangement from the 27 possibilities configurations.

5: Using the best configuration to overcome the significant noises that escort the ECG signal in all cases in general

4.3.1.1 Matlab Simulink Implementation

With MATLAB, SIMULINK version 8.2.0.701(2013b) 64 bit for windows 7, operating system OS 64bits; the project has been achieved meritoriously by retrieving the raw ECG signal from a Physiobank (PTB diagnosis ECG database).

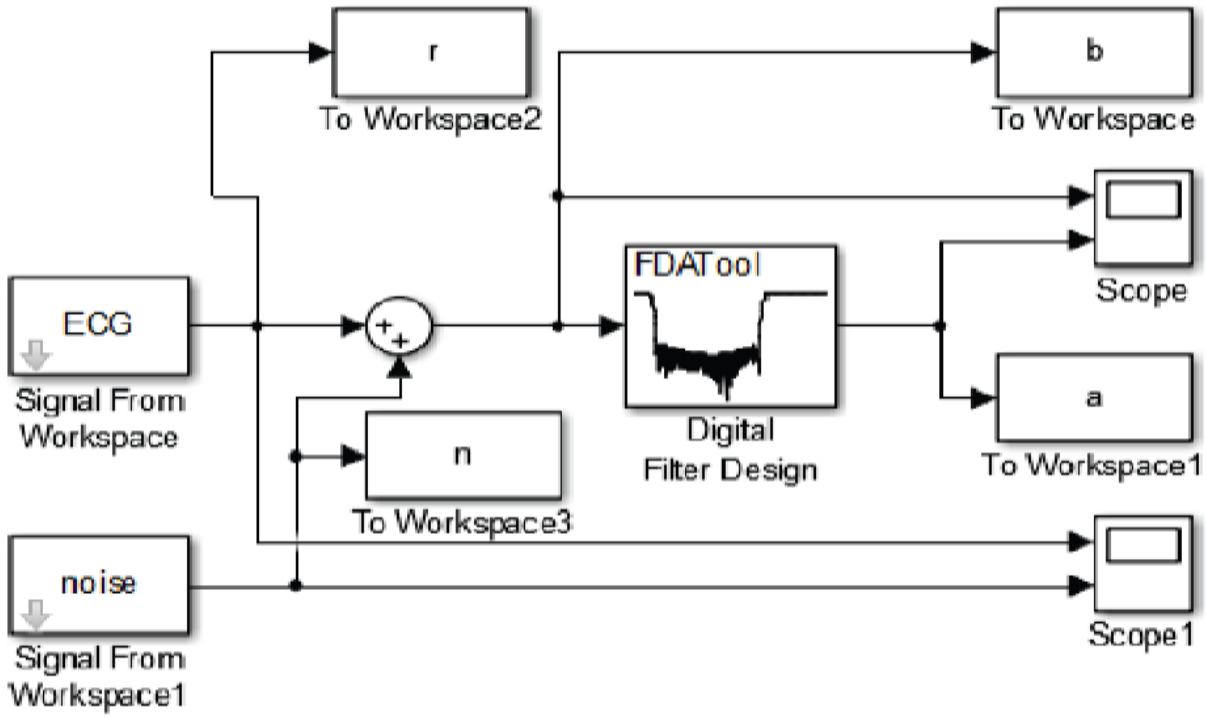

Figure 4.3 Simulink FDA Tools model used in the first stage

In the first article, our approach is divided into two stages (see Figure 4.2);in the first one, the three windows of the best performance are selected among the existing ones from FDA Tools for each type of digital FIR filter separately by using one FIR filter alone as shown in Figure 4.3 i.e. The SNR and MSE performances of this filter are tested at each time when configured it on any available window, through applying them on this filter. The comparison has been made by determining the performance of each window in each type of this filter separately so that we can get to consider the validity of the selected windows when applying them to the combination of three filters on cascade (HPF- BSF-LPF).

In the second stage, the three windows produced by the first stage are used to form the cascading FIR filter. The cascaded filters are the combination of high pass, band stop and low pass filters (HPF-BSF-LPF) respectively, thence all these filters are in a fixed order of (360)

is chosen for the de-noising ECG signal task. The three windows taken from the first stage are distributed on these three cascaded filters. Hence the disposition of these windows will produce twenty-seven possible configurations of cascaded filters, i.e. let's (FW=27) represent the cascade FIR filter configurations s, as shown in Table 4.3. Where the F is the number of filters and W is the number of windows, i.e. there are three selected windows and three filters (HPF-BSF-LPF), there will be a total of 27 cascaded FIR filter configurations. According to SNR and MSE measurements, the best configuration (BC) has been selected among all possible arrangements to generally filter the noisy ECG signals in all cases.

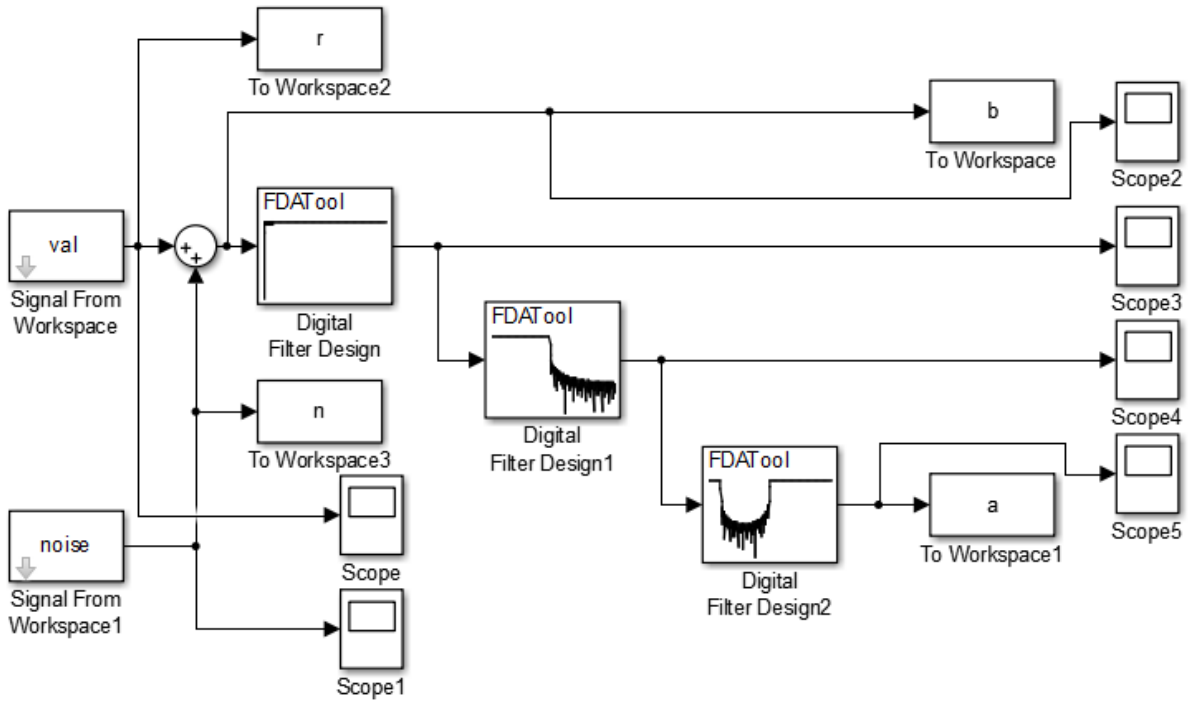

Figure 4.4 Simulink FDA Tools model used in the last stage

4.3.1.2 Results evaluation and discussion

In the first stage, the results noticed that Kaiser (K), Rectangular (R) and Taylor (T) windows are the three windows that achieved acceptable performances by comparison between their SNR and MSE assessment in HPF, BSF, then LPF separately, which were selected for the second stage experiments. As mentioned earlier, the minimum mean square error and maximum signal-to-noise ratio is the proper condition for accessing an optimal adaptive configuration algorithm to achieve the de-noising task. Therefore, the Kaiser window

significantly improved in each HPF, BSF and LPF. Furthermore, whereas the Rectangular window results were very excellent values in HPF and BSF but in BSF it is proved an acceptable result if comparing it with Kaiser and Taylor windows. On the other hand, the Taylor window has detected a high performance in BSF and satisfactory performance in LPF if compared with Kaiser and Rectangular windows; furthermore, HPF has less value than Tukey window performance, but it is satisfied.

Table4.2First stage results of several windows using SNR and MSE parameters

FDA Tools Windows	**HPF**		**BSF**		**LPF**	
	SNR	**MSE**	**SNR**	**MSE**	**SNE**	**MSE**
Barttlet	20.3240	0.0069	33.5913	0.0056	47.9247	0.0042
Bartt-Hann	19.7721	0.0070	34.5890	0.0055	47.9914	0.0042
Blackman	19.1996	0.0071	34.9675	0.0055	48.0038	0.0042
Blac-Harris	18.9564	0.0071	34.9193	0.0055	48.0041	0.0042
Bohman	19.1508	0.0071	34.8423	0.0055	47.9959	0.0042
Chebyshev	18.9991	0.0071	34.9423	0.0055	48.0035	0.0042
Flat Top	18.6690	0.0071	34.3739	0.0055	47.9689	0.0042
Gaussian	19.6787	0.0070	35.6455	0.0054	48.2133	0.0042
Hamming	19.9687	0.0070	36.1834	0.0054	48.4048	0.0041
Hanning	19.6121	0.0070	34.9235	0.0055	48.0127	0.0042
Kaiser	**26.7647**	**0.0063**	**38.8508**	**0.0051**	**54.3886**	**0.0035**
Nuttall	18.9761	0.0071	34.9283	0.0055	47.9979	0.0042
Parzen	19.0402	0.0071	34.7434	0.0055	47.9969	0.0042
Rectangular	**27.3729**	**0.0062**	**37.5115**	**0.0052**	**55.0158**	**0.0035**
Taylor	20.9328	0.0069	**39.4952**	**0.0050**	**49.2664**	**0.0040**
Triangular	20.3465	0.0069	33.6694	0.0056	47.9515	0.0042
Tukey	**21.6162**	**0.0068**	33.9052	0.0056	48.0352	0.0042

Table 4.2 shows the results obtained from the final phase of eliminating the predominant interference of the ECG signal, by applying all possible experiments to the three filters used in the pattern of the serial system (HPF, BSF and LPF),respectively.

The windows extracted from the previous stage are used in these experiments, and the outputs SNR and MSE performances are compared, which were given by each configuration, where the best-obtained results are concentrated in the first and the middle of Table 4.3 that derived according to the improved configurations respectively. Among these configurations,

the structure (R-R-R) is the best configuration that achieves better results according to the above-mentioned rules for maximum SNR and minimum MSE.

Table 4.3the last stage results in de-noising the performance of several configurations using SNR and MSE

Configuration Selecting for HPF-BSF-LPF	**Performance**		**Observed Effect**
	SNR	**MSE**	
K-K-K	24.6386	0.0065	improved
K-K-R	24.6576	0.0065	improved
K-R-K	24.9078	0.0065	improved
K-R-R	24.9287	0.0065	improved
K-K-T	24.4231	0.0065	improved
K-T-K	22.0208	0.0068	improved
K-T-T	21.8661	0.0068	improved
K-R-T	24.6849	0.0065	improved
K-T-R	22.0343	0.0068	improved
R-R-R	25.4414	0.0064	improved
R-R-T	25.1830	0.0065	improved
R-T-R	22.3860	0.0067	improved
R-T-T	22.2100	0.0068	improved
R-R-K	25.4205	0.0064	improved
R-K-R	25.1539	0.0065	improved
R-K-K	25.1337	0.0065	improved
R-T-K	22.3718	0.0067	improved
R-K-T	24.9044	0.0065	improved
T-T-T	18.0584	0.0072	Not improved
T-T-K	18.1456	0.0072	Not improved
T-K-T	19.4965	0.0070	Not improved
T-K-K	19.6093	0.0072	Not improved
T-T-R	18.1537	0.0070	Not improved
T-R-T	19.6332	0.0070	Not improved
T-R-R	19.7582	0.0070	Not improved
T-K-R	19.6192	0.0070	Not improved
T-R-K	19.7481	0.0070	Not improved

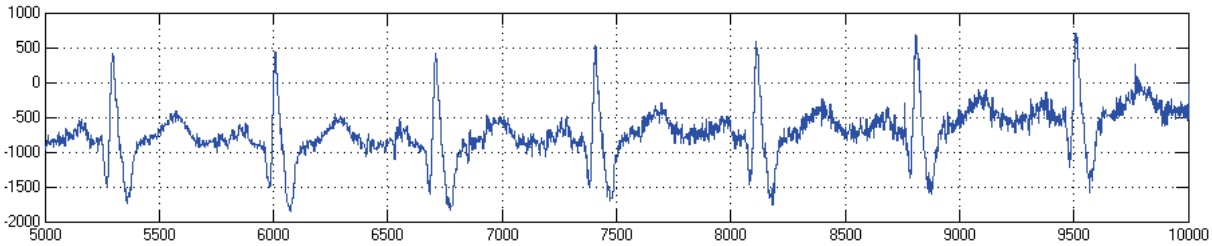

Figure 4.5 Raw ECG signal Mixed with BLW and PLI Noises

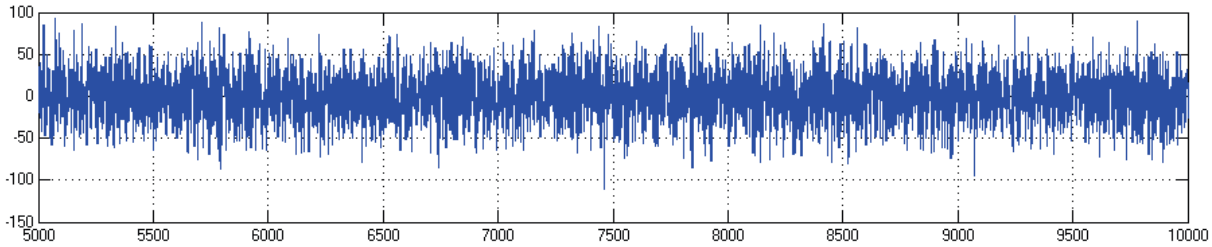

Figure 4.6 Additive WGN with SNR =-27.42 dB

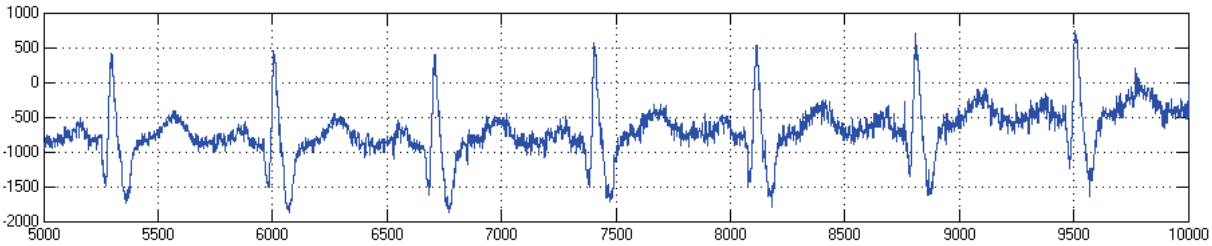

Figure 4.7 Noisy ECG signal

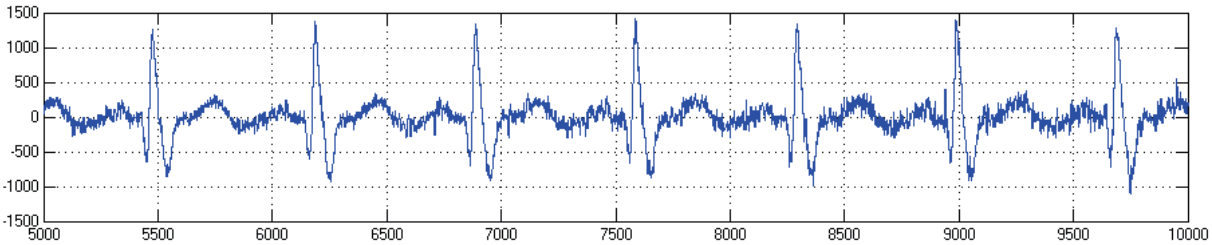

Figure 4.8 ECG signal without BLW Noise

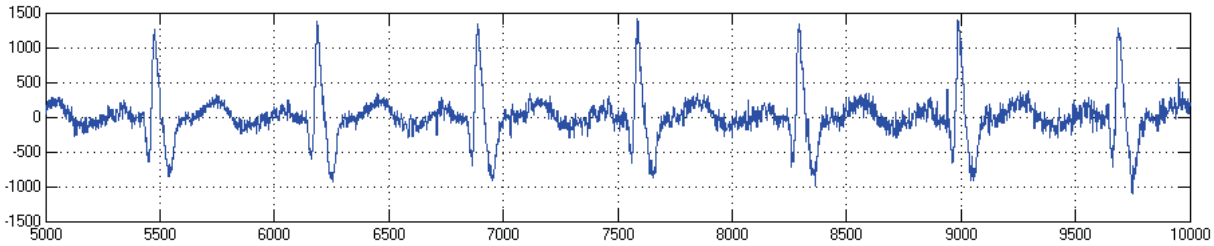

Figure 4.9 ECG signal without PLI Noise

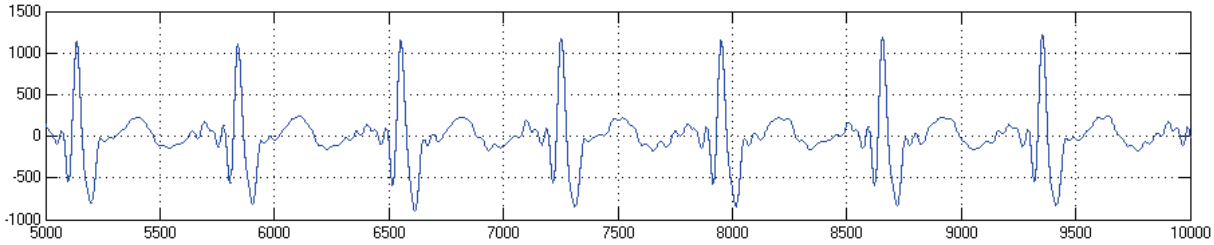

Figure 4.10 Filtered ECG signal (without EMG Noise)

Figures 4.5- 4.10 showed the Steps of de-noising ECG signal using record ID S0010_rem derived from the PTB diagnostic database.

The figures show the steps of stage 2 from the proposed method applying the BC technique in which the raw ECG signal passes during noise cancelling. Furthermore, the PTB database records contain clear ECG signals grouped with respiration effect, and 50/60 Hz effect, then added to it a WGN to form a noisy ECG signal by three major noises according to the following points.

Figures 4.5 Raw (original) ECG signal was recorded for Patient No. 001; this indication is accompanied by BLW and PLI noises, which have been diagnosed with the disease of Myocardial Infarction, refer to additional diagnoses of Diabetes Mellitus.

Figures 4.6 WGN corrupted the raw ECG signal and produced errors in the information, with an SNR=-27.42 dB adjusted to achieve SNR levels.

Figures 4.7The raw signal mixed with WGN (noisy ECG signal), which passes through three phases of filtration in tags as shown in the following signals (d, e and f).

Figure 4.8 the signal is resulting from the first filter HPF is free from BLW noise, which became according to the axis line 0.

Figure 4.9 the signal resulting from the second filter BSF is free of PLI noise (50/60Hz). Figure 4.10 the signal is resulting from the third filter LPF is free of EMG noise (de-noised ECG signal). Hence the phase response of the (R-R-R) configuration based on the FIR filter technique is linear and stable with a clean ECG signal that is free. Whereas, this filter design is shapes the signal waveform and maintains the main features of the smooth ECG signal in the desired manner; for more confirmation, see Figures. 4.15 and 4.16.

4.3.2 Evaluating the Influence of filters position in the cascaded filter

In this study, a new optimization on windowing technique based on Finite Impulse Response (FIR) filters is proposed for revealing and evaluating the Influence of filters position in cascaded filter tested on the ECG signal de-noising. As a result, baseline Wander (BLW), power line interference (PLI) and electromyography (EMG) noises are getting removed.

The performance of the adopted method is evaluated on the PTB diagnostic database. Subsequently, the comparisons are based on Signal to Noise Ratio (SNR) improvement and Mean Square Error (MSE) minimization. The Rectangular and Kaiser windows have been used for the more powerful performances. The Disparity Average (DA) of SNR values is detected; in both Kaiser and Rectangular windows are assessed by ±0.38046dB and ±0.70278dB, respectively, while the MSE values were constant.

The filtration system's excellent configuration or filters position (H-B-L) is selected according to high measurements of SNR and low MSE, too, to de-noise the ECG signals. First, this applied approach has led to SNR improvement with MSE minimization. This means that there is a significant contribution to improving the field of filtration. Figure 4.11 shows the diagram of the proposed last method with the stricture of the filtering preprocessing.

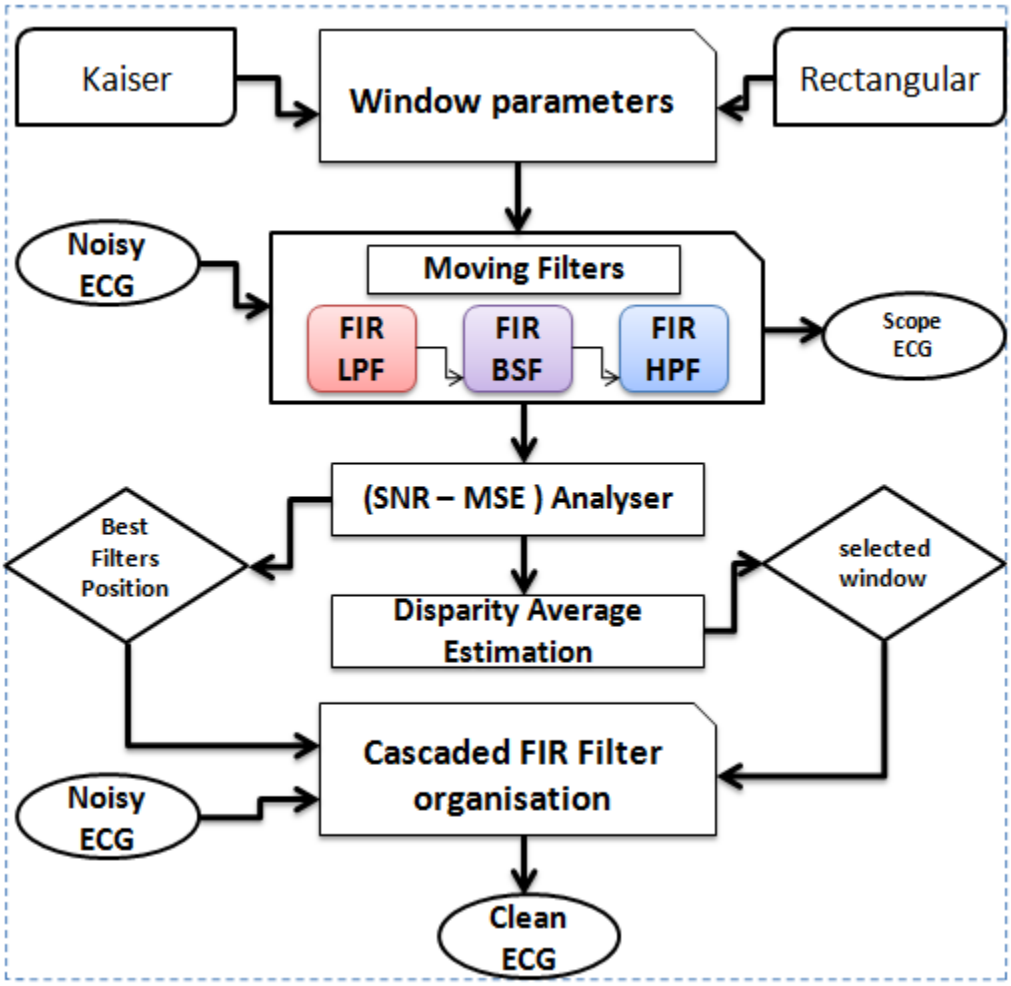

Figure 4.11 Diagram of the proposed method [2]

Algorithm Pre-Processing Captured ECG signal

Input: Noisy ECG signal *E* Input.

Output: De-noising ECG *E* Output.

Issue: an investigation into the change value of SNR end MSE performances in terms of changing the position of the filters.

1: Load *E* Input.

2: Initialization of each filter by choosing orders, cut-off frequency and simple frequency in FDA Tools.

3: Filtering *E* Input signal by using (Kaiser window, then Rectangular window) available in FDA Tools, and changing the position of the filters each time.

4: Computing and comparing the *E* Output according to SNR and MSE parameters for the position of each cascaded filter.

5: Disparity Average estimation of any change in the SNR or MSE values and comparing them for both windows.
6: Using the best position of filters and the best window to improve the ECG signal in all cases.

Normal and abnormal ECG signals are collected from the Physiobank database, freely available online at [15], where you can find many previously recorded ECG patterns such as a text header file, binary annotated file, and binary data signal file. Furthermore, the recorded signals have been retrieved from Physiobank ATM - export signals as (mat) format to take experiment, manipulation and implement using MATLAB and SIMULINK environments. As a proof of concept of this study, the four following subsections are included in completing the results of the experimentations [2].

4.3.2.1 ECG De-noising performance based on filters positions

Etiology of the electrocardiogram (ECG) signal allows physicians to understand the physical and pathological conditions of the ECG diagnosis. Generally, the noises can hide and corrupt important information from the beginning of heartbeat monitoring records. Some frequency noises have existed in the frequency band of the ECG signal, and the ECG signal will often get distorted, which limits the extraction of useful information from it.
The instrumentation noise refers to the noise that originated in the data collection device, the electronic noise, which is a specific kind of instrumentation noise. This kind of noise is called flicker noise which overlaps in the frequency domain with electromyography (EMG) noise. Therefore, filtering the EMG noise will, in turn, reduce these flickers [18]. Other noise sources affecting the ECG signal include channel noise, electrode contact noise, motion artefacts….etc.
To the best of our knowledge, no single study proves or disapproves of the impact of filters position on the performance of the cascading filter. To address this issue, a new proposed approach to prove the impact of the filters arrangement with employee the Kaiser and Rectangular window distributed on the cascading FIR filter, i.e. select the accuracy configuration that gives the best outputs performances of SNR and MSE for each filter position in each window.
The Kaiser and Rectangular windows were selected from FDA Tools since they're largely used in more than one work related to filtering the ECG signal and their performance as it

appears in [19]. and [20]. This procedure will apply to each type of digital FIR filter, as shown in Figure 4.12. On the one hand, the SNR and MSE performances of each configuration produced by changing the filter positions, which are used to form the cascading FIR filter, we are compared with the results of Rectangular and Kaiser windows performances.

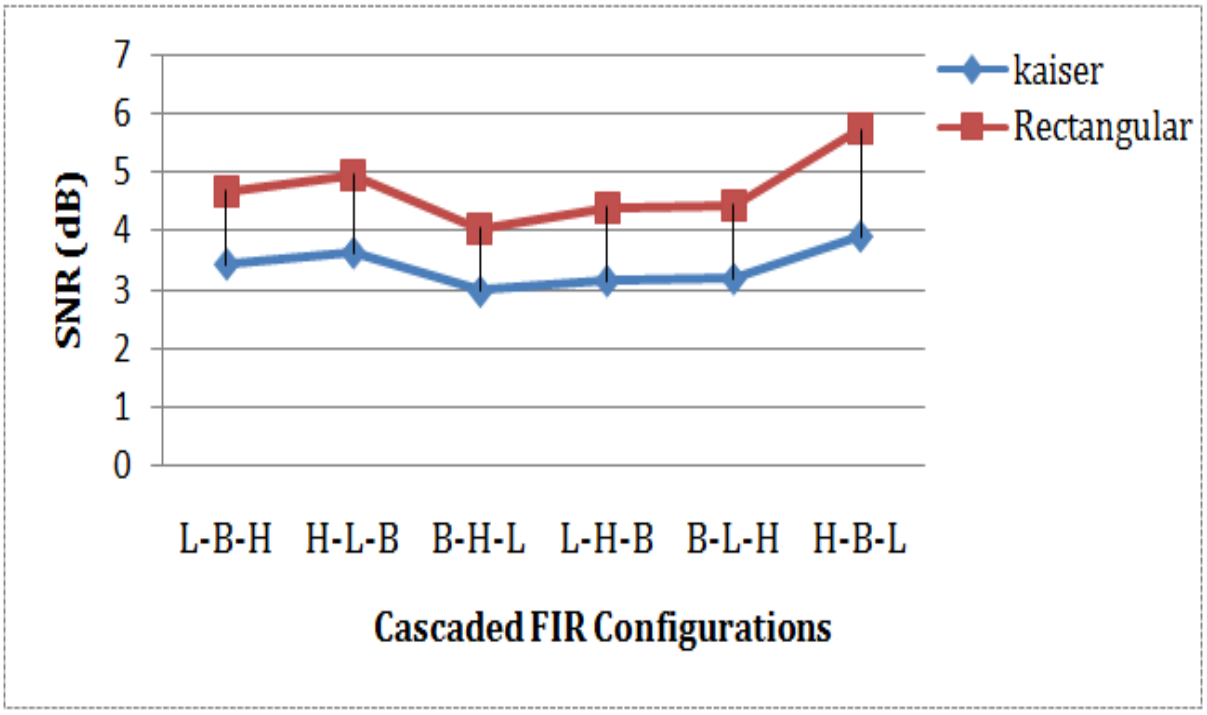

Figure 4.12 The Kaiser and Rectangular performances [2]

The cascaded filters are taken with a fixed order of (360), because this approach is limited to studying the change in the system performance by changing the positions of its constituent filters, and this is what makes the observed stationary measurements in all possible attempts. However, the method based on estimating the disparity of the changed value in SNR and MSE performances, resulting from the output of cascade filter bloc design, will be produced six possible patterns of cascade filter, i.e. it's represented the six cascaded filter configurations for each mentioned window as shown in Table 4.6, i.e. The two windows from FDA Tools, are tested with the filters. As a result, the six cascaded filter configurations are obtained.

According to the condition of SNR and MSE measurements, the disparity average (DA) is detected from changing values of filters position patterns; we will be investigating the best filter position and the convenient window applied to achieve the task of filtering the noisy

ECG signals in different cases. The position of the three filters that justified the best configuration had to achieve a more potent increase in the quality and accuracy of the ECG signal.

On the other hand, more than 10recordedsamples used in advance, by taking into account more than one diagnosis of different heart diseases [15]. Hence, the results are inserted in Table 4.4 which shows the estimation of the SNR and MSE obtained from the final phase of eliminating the predominant interferences of the ECG signal before and after filtration.

Figure 4.14 illustrates a detailed work plan that lists the steps identified to reach the desired results. For clarification only, here we find the term moving filter (cascaded FIR filter), which means that the filters are repositioned simultaneously inside the cascaded filter every time from making the necessary measurements. The following steps illustrate the algorithm procedure.

4.3.2.2 Results evaluation and discussion

Table 4.4shows the results from the final phase of eliminating the predominant interference of the ECG signal. First, apply all possible experiments on the three filter positions representing the cascaded FIR filter for the serial system. Then, the outputs SNR and MSE parameters given by each configuration (position) are compared in Kaiser then Rectangular window. Hence, the test of various SNR levels are concentrated (2 to 6 dB), where the best SNR levels are trapped nearly like 3.40< SNR<3.90 dB in the Kaiser window and 4.95< SNR< 5.75 in the Rectangular window[2].

Table 4.4 the results of the de-noising performance of several positions using SNR and MSE parameters

Filters positions	Kaiser		Rectangular	
	SNR	MSE	SNR	MSE
L-B-H	03.4351	0.0100	04.6830	0.0098
H-L-B	03.6239	0.0100	04.9433	0.0098
B-H-L	02.9798	0.0100	04.0432	0.0098
L-H-B	03.1553	0.0100	04.3981	0.0098
B-L-H	03.1891	0.0100	04.4268	0.0098
H-B-L	03.8996	0.0100	05.7223	0.0098
DA	±0.38046	0	±0.70278	0

The disparity average of SNR values in Kaiser and Rectangular windows are estimated by ±0.38046 dB and ±0.70278 dB. These values have been extracted to identify the difference between these windows. Moreover, which gets up the task of choosing the right window is possible.

These values may be small but can affect the quality of the process and the appearance of the morphology of ECG signals as shown in Figures 4.13 and 4.14. However, the MSE performances remained stable in both windows, as derived from improved configurations. Thus, observations admitted the (HPF-BSF-LPF) configuration or H-B-L position as the best among all positions; moreover, this structure achieves the desired accuracy to improve the quality of ECG signals through the rules mentioned above of maximum SNR and minimum MSE. However, such as found in the following table the results achieved from this composition after generalizing the validity of its performance on many signals with different sources and patterns.

You can look at the points represented in the graphical curve of the performance of the used windows. By checking what is shown, the values of SNR are constantly changing in each configuration that has been applied. As the values were reasonably consistent, except for the Rectangular as a fixed window, it achieved a noticeable rise in the H-B-L configuration, which supports what was stated in the comment in Table 4.4. From here, it will be better to contain the variables that can be examined through the ANOVA application.

4.3.2.3 The ANOVA results

To check the validity of results, the one-way analysis of variance (ANOVA) was also employed for analyzing the effects of filter position with the two selected window types at various SNR values on the ECG de-noising system. The ANOVA results ($F = 22.993$, $P = 0.000$) indicate that the filters' position arrangement of the cascaded system at various ECG signals has significant differences [2].

4.3.2.4 ECG De-noising based on H-B-L configuration

Figure 4.13 shows the steps of the cascaded FIR filter of our proposed method, in which the signal passes during noise cancelling. Furthermore, the PTB database records contain clean ECG signals grouped with respiration and 50/60 Hz effects, and the WGN has been added to form a noisy ECG signal by three major noises, as shown in Figure 4.14.

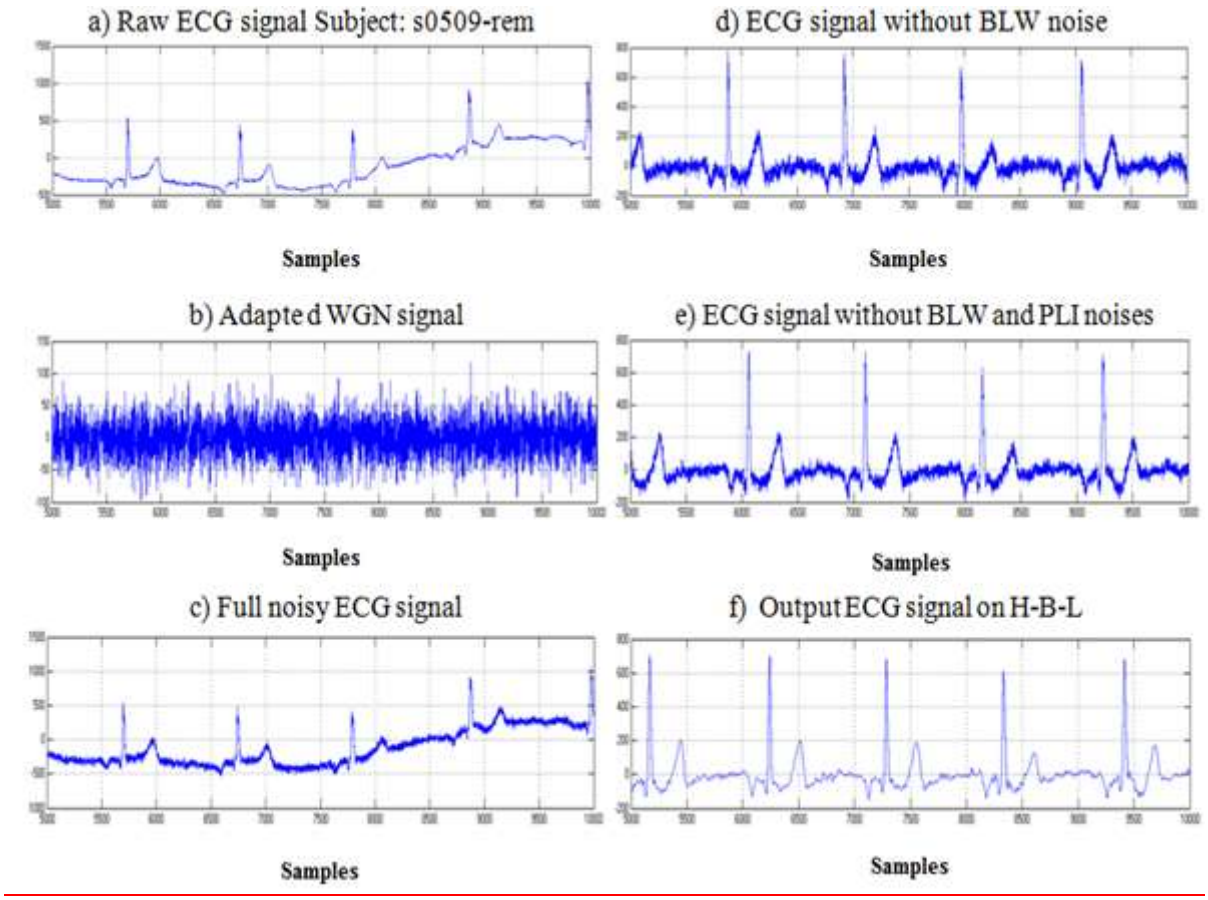

Figure 4.13 Steps of de-noising ECG signal using the H-B-L configuration[2].

The H-B-L configuration to be proved a successful noise removal procedure while preserving the morphology of the ECG signals. However, you can check the signal as it goes through the following filtering steps. Where,

a) Raw (original) ECG signal was recorded for Patient N^{o} 271 in the PTB database; this indication is accompanied by BLW and PLI noises, which have been diagnosed with the disease of Myocarditis, and that's due to additional diagnoses of Arterial Hypertension[15].

b) WGN corrupted raw ECG signal at an SNR of -27.42 dB adjusted to achieve SNR levels. It is used as the muscles' contraction effect source, i.e. the effect of EMG noise [21].

c) The raw signal mixed with WGN (full noisy ECG signal) passes through the subsequent three phases of filtration in tags as shown in the following steps. d, e and f.

d) The signal resulting from the first filter HPF is free from BLW noise, where it became following the axis line 0.

e) The signal resulting from the second filter BSF is free of BLW and PLI (50/60Hz) frequency noises, which should be input for the next stage of the de-noising task.

f)The signal resulted from the third filter LPF and the EMG noise was removed with the other noises (de-noised ECG signal).

4.3.2.5 ECG De-noising based on the comparison of the morphologies of deferent configurations

By applying the different configurations, in which a noticeable difference was created out on the ECG signal morphology. The signals generated by this work show the difference between the cases. Where the resulting ECG signal was presented as the real signal waveform. Hence, a),b),c),d),e), and f) illustrate the morphology of the cardiac cycles, with different thicknesses in each of them, but f) It is the best due to the excellent configuration (H-B-L). However, the resulting signal preserves the ECG morphology. Hence, in this type of studied data, we found that the P wave was inverted (negative) [22]due to the diagnostic status of the patient from which the data are drawn.

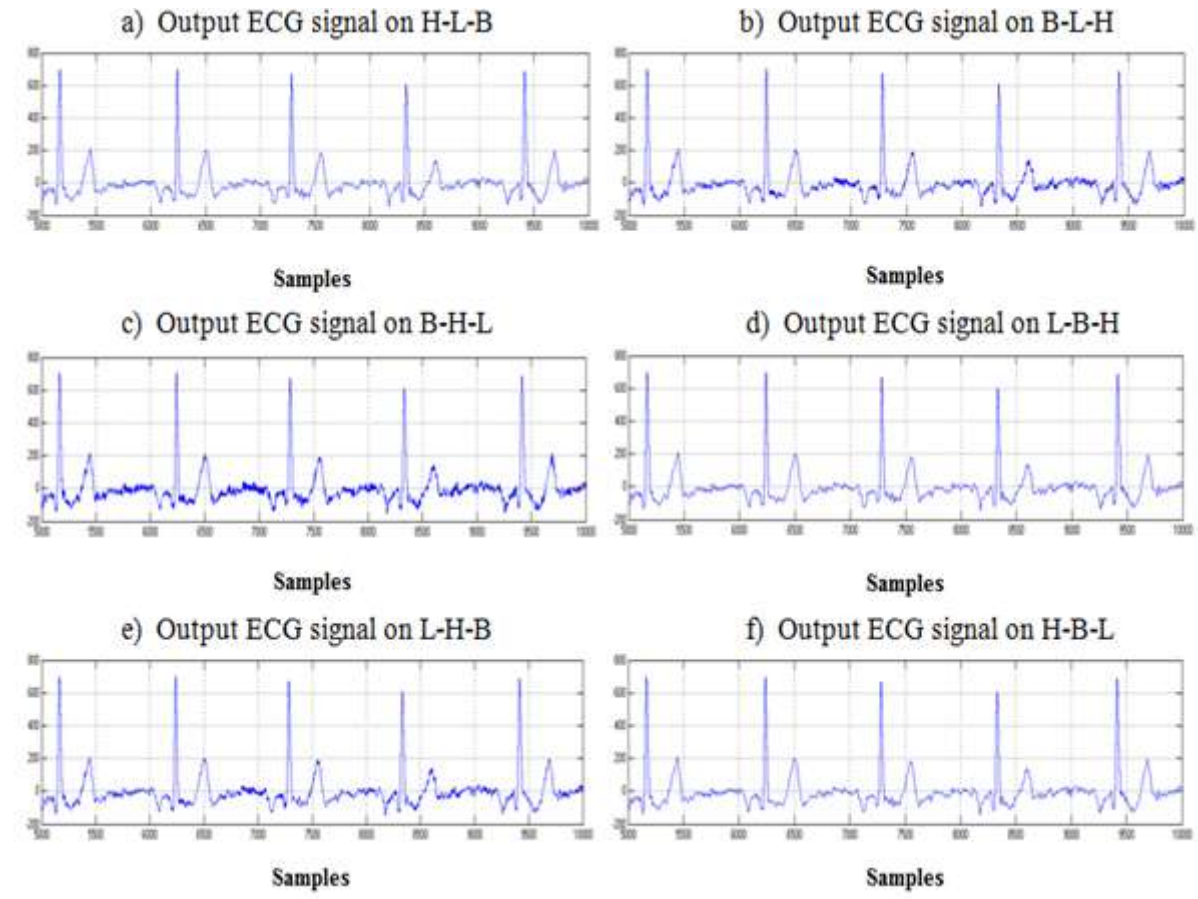

Figure 4.14 the output signals resulted from the cascaded filter with different configurations

4.4 Confirmation on other ECGs diagnostic class

The results obtained in Table 4.5from the conformations of our proposed approaches using the (H-B-L) configuration with the selected Rectangular window.

Table 4.5 Confirmation effects of the de-noising performance of a proposed method for PTB diagnostic database for different diseases

Diagnostic class	PTBdb	SNR_1	SNR_2	MSE_1	MSE_2	Effect on waveform
Myocardialinfarction	S0175_rem	5.1806	19.8621	0.0092	0.0072	Smooth signal
	S0010_rem	-5.8159	25.4414	0.0087	0.0064	Smooth signal
Cardiomyopathy	S0392 lrem	-3.0643	13.0686	0.0100	0.0087	Smooth signal
	S0200_rem	-2.3932	05.6751	0.0097	0.0092	Smooth signal
Heart failure	S0023_rem	-10.177	06.7796	0.0099	0.0093	Smooth signal
	S0183_rem	-0.3146	12.3121	0.0101	0.0089	Smooth signal
Bundlebranch block	S0441_rem	-7.1860	23.0859	0.0111	0.0088	Smooth signal
	S0429_rem	-1.9127	09.3006	0.0107	0.0098	Smooth signal
Dysrhythmia	S0018_rem	-3.3716	11.2205	0.0105	0.0094	Smooth signal
	S0169_rem	-3.1767	03.4769	0.0097	0.0093	Smooth signal
Myocardialhypertrophy	S0390_rem	-3.1767	03.4769	0.0097	0.0093	Smooth signal
	S0434_rem	-11.383	07.7710	0.0095	0.0088	Smooth signal
Valvular heart disease	S0030_rem	-8.7241	18.8872	0.0103	0.0084	Smooth signal
	S0199_rem	-8.4363	10.4248	0.0093	0.0083	Smooth signal
Myocarditis	S0509_rem	01.5051	05.7223	0.0103	0.0098	Smooth signal
	S0510_rem	-5.6683	04.4123	0.0102	0.0098	Smooth signal
Healthy controls	S0545_rem	-5.4696	01.9337	0.0104	0.0103	Smooth signal
	S0500_rem	01.4517	01.8169	0.0107	0.0105	Smooth signal

Table 4.5 shows the results obtained from the conformations of our proposed approach configuration. The records shown in this table are extracted from the PTB diagnostic database; within the header (.hea) files of most of these ECG, records contain a detailed clinical summary, including diagnosis, age, gender, medical history data, hospital medication and interventions [15]. The medical precis isn't to be had for 22 topics. The diagnostic lessons of the ultimate 268 topics are summarized in chapter two of this thesis.

The $SNR_1$and MSE_1 represent the estimations of ECG records before filtration, and the SNR_2 and MSE_2 represent the estimations after filtration.

The proposed approach, which employs the different window functions and different FIR filters under the condition of maximum SNR and minimum MSE, detected that the ECG

signal enhancement had been achieved with notable performances in each diagnostic record class and smooth output signals.

However, in the context of this thesis manuscript, the proposed methods are proved that they are can eliminate the problem of determining the appropriate window for any filter to get read the undesired frequencies from any raw signal.

Therefore, the window technique should not be random due to its impact on the resulting signal quality. Each type of window, whether a fixed or adjustable window, has its characteristics, mainly if used to implement the cascaded filter.

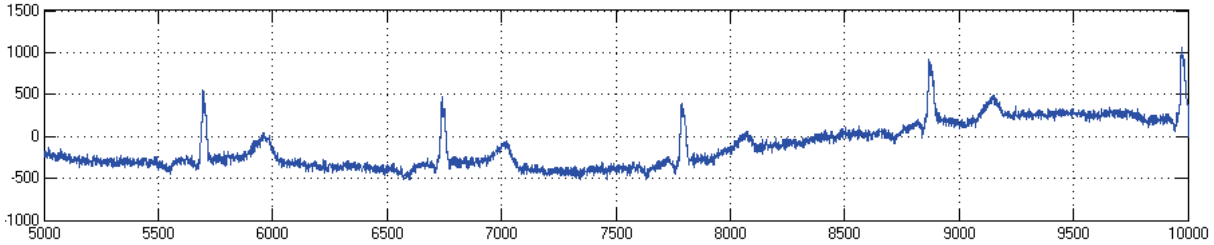

Figure 4.15 Raw ECG signal before filtration

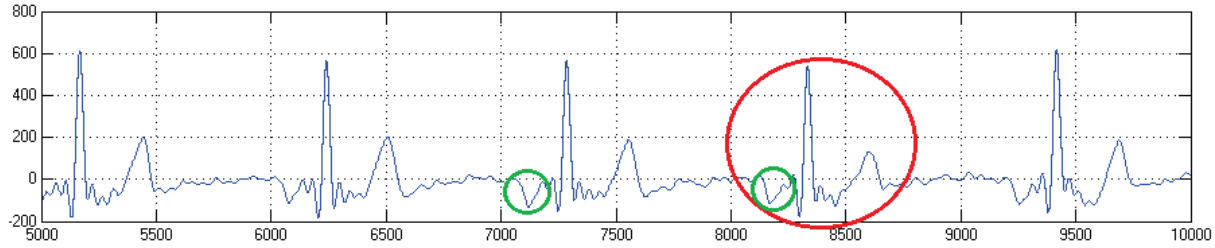

Figure 4.16 ECG signal after filtration

Figures 4.15 and 4.16 represent the record ID: S0509_rem before and after filtration. The raw (original) ECG signal was recorded for Patient No271 in the PTB database; this indication is accompanied by BLW and PLI noises, which have been diagnosed with the disease of Myocarditis, and that's due to additional diagnoses of Arterial Hypertension [15]. Where the resulting ECG signal was presented as the real signal waveform. Hence, the red circle illustrates the morphology of one cardiac cycle; the green circles show the P wave; however, the P wave was negative.

4.5 Comparison of the proposed approach with existing works

The high performance obtained in this optimization has been compared with the existed papers, [19] and [23]. Hence, this comparison contains four types of ECG databases from the Physiobank ATM. So, the significant SNR improvement and MSE minimization resulting from the different proposed cascade filter designs, are illustrated in Table 4.6.

Table 4.6 comparison of proposed cascaded fir filter design with existing work

Author name	Physio-Bank ATM database	SNR improvement after filtering(dB)	MSE minimization (%)
Patro et al., 2015 [192]	MIT-BIH NSR DATA	4.14	21.81
	MIT-BIH ECG ID DATA	2.47	35.30
Navdeep et al., 2019 [203]	MIT-BIH Arrhythmia	7.75	-
Present work	PTB diagnostic ECG database	31.2573	26.43

Firstly, this study deals with the problem of ECG denoising in the serial filter, mainly due to the lack of awareness of their importance in previous works. This method of selecting the best configuration of the cascaded filter used to remove noise has achieved fairly impressive success in terms of the quality of performance and the appearance of the resulting signal. Secondly, after an in-depth analysis of the data obtained, we reach that this task gives valuable and additive contributions in successive filtering. Finally, the algorithm preserves useful information while removing noises from the ECG signal, with the performance of noise reduction being outstanding [2].

4.6 Results and Discussion

In this chapter, we have proposed an alternative method for building a cascaded FIR filter to enhance the ECG signal quality through two methods.

Every earlier research may agree that the cascaded filter can be applied as a design for suppressing multi-noises from ECG signals, but if it can save the morphology of the signal. With the deep study, the capability of the proposed approaches technique was identified and evaluated using the potential of SNR and MSE parameters. Therefore, the overall results show that selected filters and windows are a reliable technique to recognize the various effects of

cascaded filter design. The experimental results are shown that the Rectangular window is more potent than the other windows. Hence, the best SNR levels are trapped nearly like 3.40 dB < SNR< 3.90 dB in Kaiser Window and 4.95 dB < SNR< 5.75 dB in the Rectangular window. Hence, the disparity average of SNR values in Kaiser and Rectangular windows are estimated by ±0.38046 dB and ±0.70278 dB, respectively. However, the MSE performances have remained stable or the difference is minimal.

On the other hand, this approach has led to 31.30 dB SNR improvement with MSE minimization of 26.43%. So, the objectives of this study have been successfully achieved with the desired expectations, even by using more than ECG's signal with incorporating different diagnostic classes. The excellent configuration or filters position (H-B-L) was proved to be a successful de-noising action with saving the morphology of ECG signals. This optimization will undoubtedly provide an efficient additional tool in ECG signal analysis, where the filter configuration plays a vital role in significantly improving the cascaded filter performance. Moreover, an extension to implementing this method in specific hardware co-simulation environments is recommended [1] [2].

Through the questions that were previously posted in section(4.1) of this chapter, which were answered in the first and second articles, which include choosing the type of window and locating of each filter in the cascaded filter block, we reached important results in the field of improving biomedical signals.

4.7 Extensions to the Embedded System using FPGA implementation

4.7.1 Introduction to the XILINX ZedBoard

Digilent's ZedBoard is a cost-effective development board for the fully programmable SoC (AP SoC) Xilinx Zynq-7000. This board contains all the elements required to create a design based on Linux, Android, Windows or any other operating system/real-time operating system (RTOS). Additionally, multiple expansion slots expose the processing system and programmable logic I/O for easy user access.

The ZedBoard is compatible with the SDSoC™ environment. The SDSoC development environment provides a familiar embedded C/C++ application development experience, including an easy-to-use Eclipse IDE development environment and a comprehensive design environment for heterogeneous Zynq SoC APs.

A frequent response to seeing the panel is that the separation community around the Zynq device appears like an intentional megastar pattern. While this fashion used to be supposed for the placement of components, it used to be for a function, no longer form. This file focuses on the electricity system's low-cost functions, which consist of the separation network. ZedBoard permits hardware and software program builders to create or consider Zynq™-7000 architectures for all programmable SoCs [24].

This assessment and improvement platform's expandability makes it best for fast prototyping and proof-of-concept development. The ZedBoard consists of Xilinx XADC, FPGA Mezzanine Card (FMC), and Digilent Pmod™ well-matched growth headers as correctly as frequent points used in device design. ZedBoard allows embedded computing functionality through Flash memory, DDR3 memory, general-purpose I/O, gigabit Ethernet, and UART technologies. [24].

The ZedBoard is a comparison and improvement board based on the Xilinx ZynqTM-7000 All Programmable SoC (AP SoC). Combining 85,000 Series-7 Programmable Logic (PL) cells with a twin Corex-A9 Processing System (PS), for wide use in many applications, the Zynq-7000 AP SoC can be targeted. Moreover, the ZedBoard's sturdy combination of onboard peripherals and growth abilities make it the best platform for each skilled designer and novices.

The ZedBoard provided the following features :

• Xilinx® XC7Z020-3CLG484C Zynq-7000 AP SoC

- Primary configuration = QSPI Flash
- Auxiliary configuration options

-Cascaded JTAG

-SD Card

• Memory

- 512 MB DDR3 (128M x 32)
- 256 Mb QSPI Flash

• Interfaces o USB-JTAG Programming using Digilent SMT1-equivalent circuit

-Accesses PL JTAG

-PS JTAG pins connected through PS Pmod

- 10/100/1G Ethernet
- USB OTG 2.0
- SD Card
- USB 2.0 FS USB-UART bridge
- Five Digilent Pmod™ compatible headers (2x6) (1 PS, 4 PL)
- One LPC FMC
- One AMS Header
- Two Reset Buttons (1 PS, 1 PL)
- Seven Push Buttons (2 PS, 5 PL)
- Eight dip/slide switches (PL)
- Nine User LEDs (1 PS, 8 PL)
- DONE LED (PL)

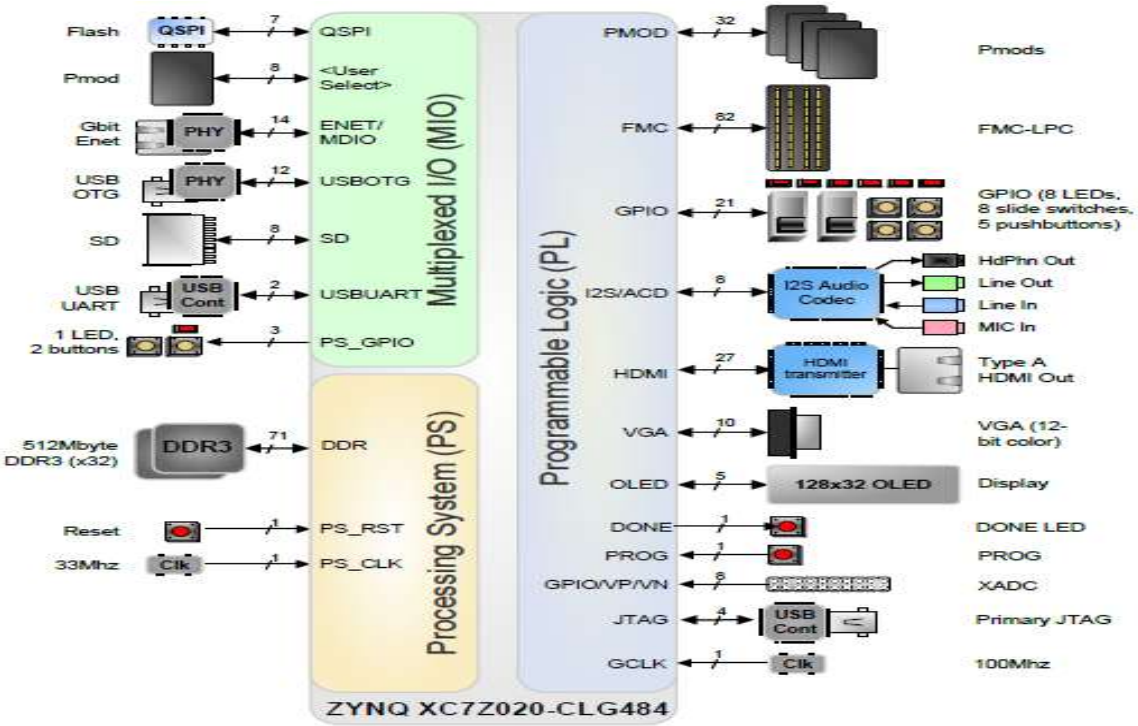

Figure 4.17 ZedBoard Block Diagram [24].

• On-board Oscillators

- 33.333 MHz (PS)
- 100 MHz (PL)

• Display/Audio o HDMI Output

- VGA (12-bit Color)
- 128x32 OLED Display
- microphone, Line-out, headphone, Audio Line-in

• Power

- On/Off Switch
- 12V @ 5A AC/DC regulator

• Software

- ISE® WebPACK Design Software
- License voucher for ChipScope™ Pro locked to XC7Z020.

4.7.2 Programmable SoC

The ZedBoard features a Xilinx Zynq XC7Z020-1CLG484 All Programmable SoC (AP SoC). Initial ZedBoards had been marked ' Rev C' and shipped with Engineering Sample "CES" grade silicon. Later ' Rev D' shipments switched to manufacturing "C" grade silicon once these grew to become available. The Zynq-7000 AP, SoC phase markings, point out the silicon grade. [24]

4.7.3 Installation and Usage

This Getting Started Guide will define the steps to set up the ZedBoard hardware. It files the technique to run a simple Linux design to exhibit a Linux utility strolling on the ARM® dual-

core Cortex™-A9 MPCore™ Processing System (PS) and interacting with the tightly coupled 7 sequences 85K Programmable Logic (PL) cells. Xilinx Embedded Development equipment is additionally added to the place the diagram can be constructed from scratch and customization choices can be discovered. If Xilinx ISE Web PACK or Design Suite software program is no longer already installed, similarly assets to set up the software, get up to date and generate a license is supplied in Appendix I.

The ZedBoard SD card is preloaded with an instance open-source Linux builds with a RAM disk file system. This file used to be created by the use of a host PC strolling Windows 7 and the directions contained would observe immediately to a Windows 7 host PC. See Appendix III for an instance of how to join a Linux host PC to ZedBoard. It is also advocated that the host PC have a wired (RJ-45 connector) Network Interface Card (NIC) that can function at 100 Mbps or a thousand Mbps.

4.7.4 Hardware ZedBoard Setup

1. Connect 12 V electricity supply to a barrel jack (J20).
2. Connect the USB-UART port of ZedBoard (J14) which is labelled UART to a PC by the use of the Micro USB cable.
3. Insert the 4GB SD card blanketed with ZedBoard into the SD card slot (J12) on the underside of the ZedBoard PCB. This SD card comes preloaded with a demo software program and incorporates a primary Linux configuration used to implement the demos listed in the later sections.
4. Verify the ZedBoard boot (JP7-JP11) and MIO0 (JP6) jumpers are set to SD card mode as described in the Hardware Users Guide.
5. Turn the power switch (SW8) to the ON position. ZedBoard will have energy on, and the Green Power Good LED (LD13) should illuminate.
6. The PC may also pop a communication container asking for driver installation.

ZedBoard has a USB-UART bridge primarily based on the Cypress CY7C64225 chipset. This function requires that a USB driver be set up on your Host PC.

If Windows acknowledges the USB-UART and masses the software program driver, then amber LED D6 will light. Please omit beforehand to the subsequent section. However, if the host PC no longer apprehend the USB-UART and enumerates it as a COM port gadget, refer

to the " ZedBoard_USB-UART_Setup_Guide.pdf" report in the hyperlink under for directions on putting in this driver. When the driver set-up is complete, proceed to the subsequent step.

8. Wait approximately 15 seconds. The blue Done LED (LD12) should illuminate, and a default image will be displayed on the OLED (DISP1).

9. Use Device Manager to determine the COM Port.

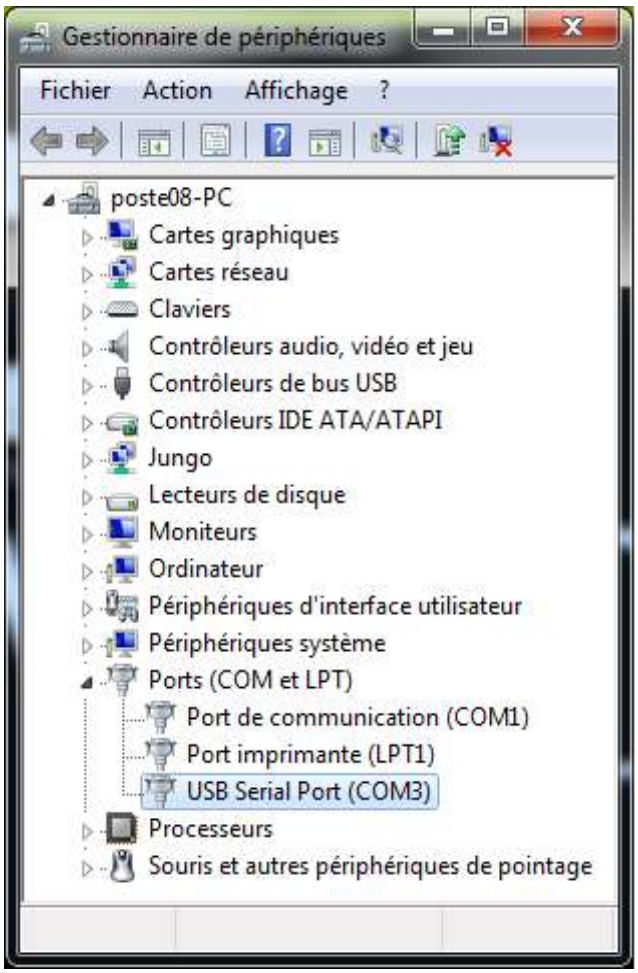

Figure 4.18 Device Managers Showing Enumerated USB-UART as COM3

10. To enable 'Port Persist' mode, double click on the "USB Serial Port (COMx)"or "Cypress Serial (COMx)"port under "Ports (COM & LPT)". Next, select the "Port Setting" tab. Finally, click the "Advanced" button.

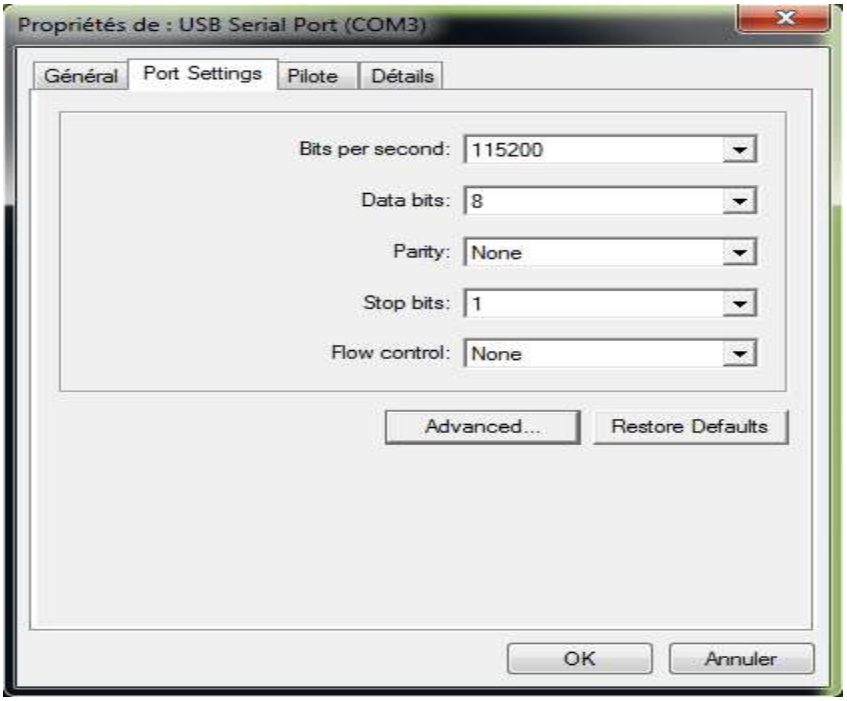

Figure 4.19 USB Serial Port Properties Dialog Box

11. Check the "Enable Port Persist" takes a look at the container in the Advanced Settings talk box. Click OK to shut the Advanced Settings communicate field and once more to shut the Serial Port Properties box. The Port Persist property needs to be enabled the subsequent time the serial port is opened.

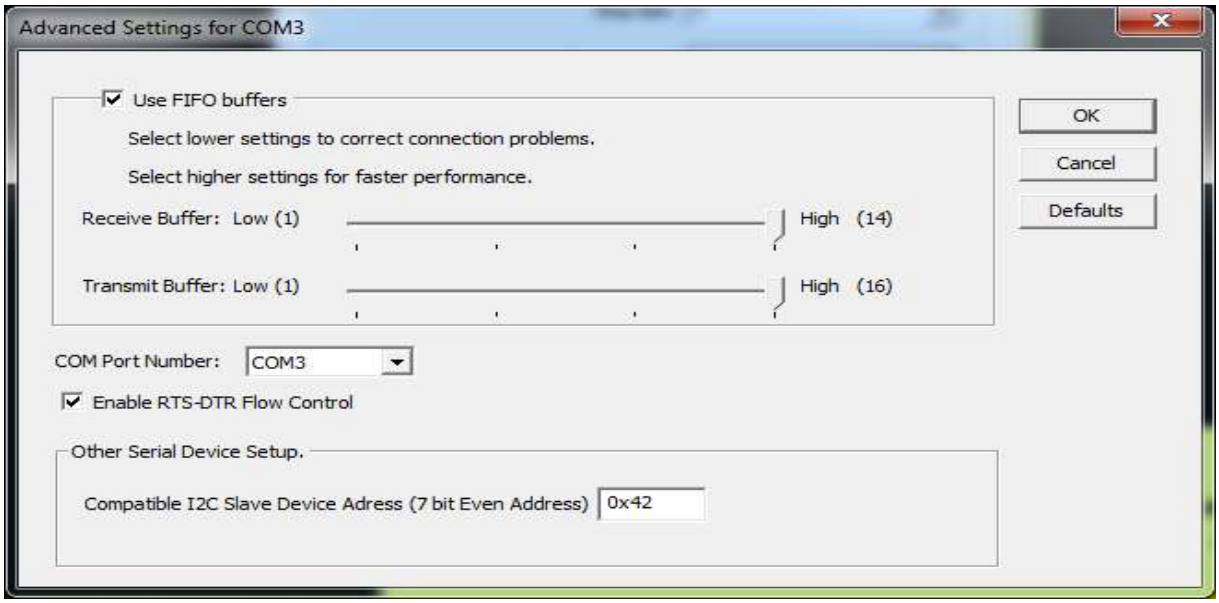

Figure 4.20 USB Serial Port Advanced Settings DialogueBox

12. On your PC, open a serial terminal program. For this demo, Windows 7 used to be used which does no longer come with a built-in terminal application. Tera Term was once used in this instance, which can be downloaded from the Tera Term undertaking on the SourceForge Japan page: ttssh2.sourceforge.jp

13. Once Tera Term is installed, Tera Term can be accessed from the laptop or begin menu shortcuts.

14. To configure baud fee settings, open the Serial Port Setup window from the Setup then Serial port menu selection. Next, select the USB-UART COM port enumeration that suits the checklist located in Device Manager. Also set the Baud rate alternative to 115200, the Data width alternative to 8-bit, the Parity choice to none, the Stop bit alternative to 1 bit, and the drift manage to none. Finally, assign the transmit prolong parameters to 10 msec/char and a hundred msec /line, and then click OK.

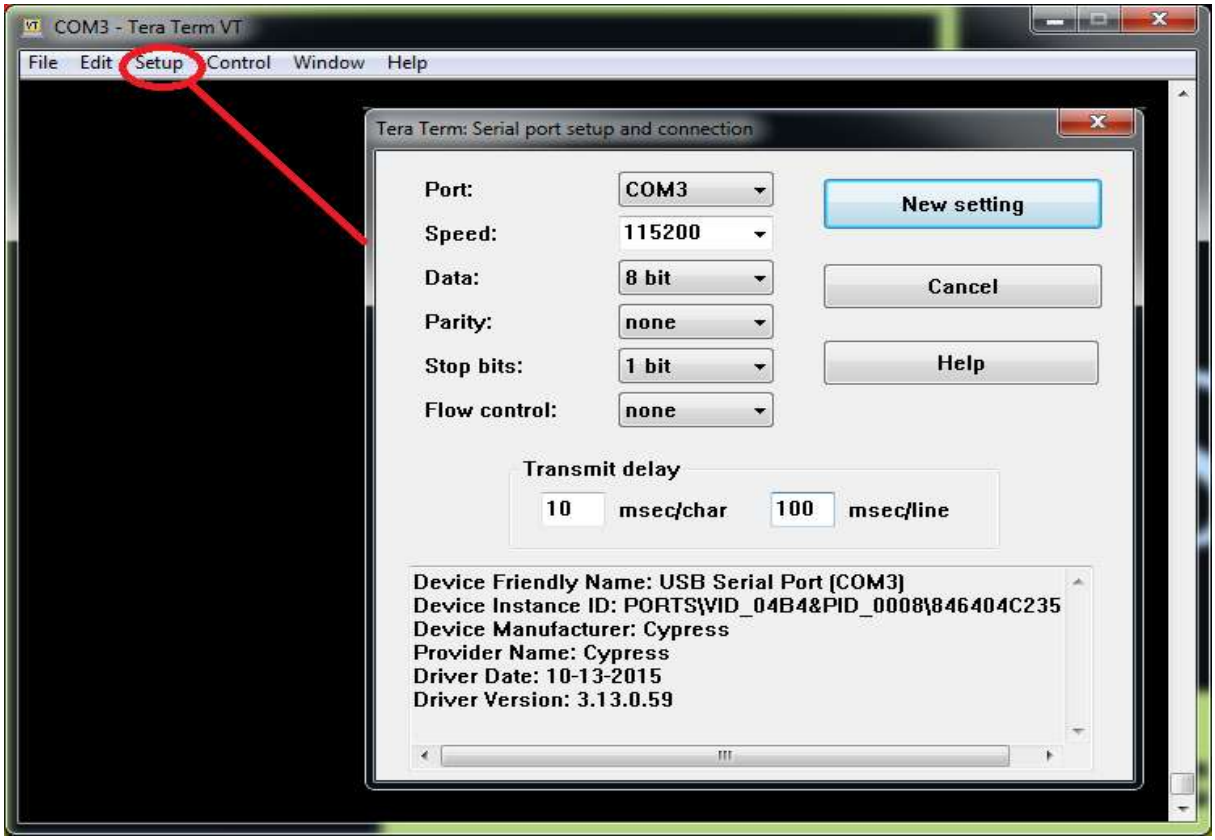

Figure 4.21 Tera Term Serial Port Setup Settings

15. Optionally, at this point, the terminal settings can be saved for later use. To do this, use the Setup and Save setup menu determination and overwrite the present TERATERM.INI file.

16. If the amber USB-Link Status (LD11) does no longer flicker to point out activity, test the driver set up to decide if the gadget driver is diagnosed and enumerated effectively and that there are no mistakes pronounced with the aid of Windows.

4.7.5 Linux Startup and Shutdown

1. Cycle electricity as soon as turning the electricity change (SW8) from ON to OFF and then returning ON.
2. In the Terminal Window, an easy Linux photograph ought to boot with performance that demonstrates the fundamental skills of ZedBoard.
3. When you have finished the usage of Linux, run the command power-off and then change off ZedBoard employing positioning the strength change (SW8) from ON to OFF.

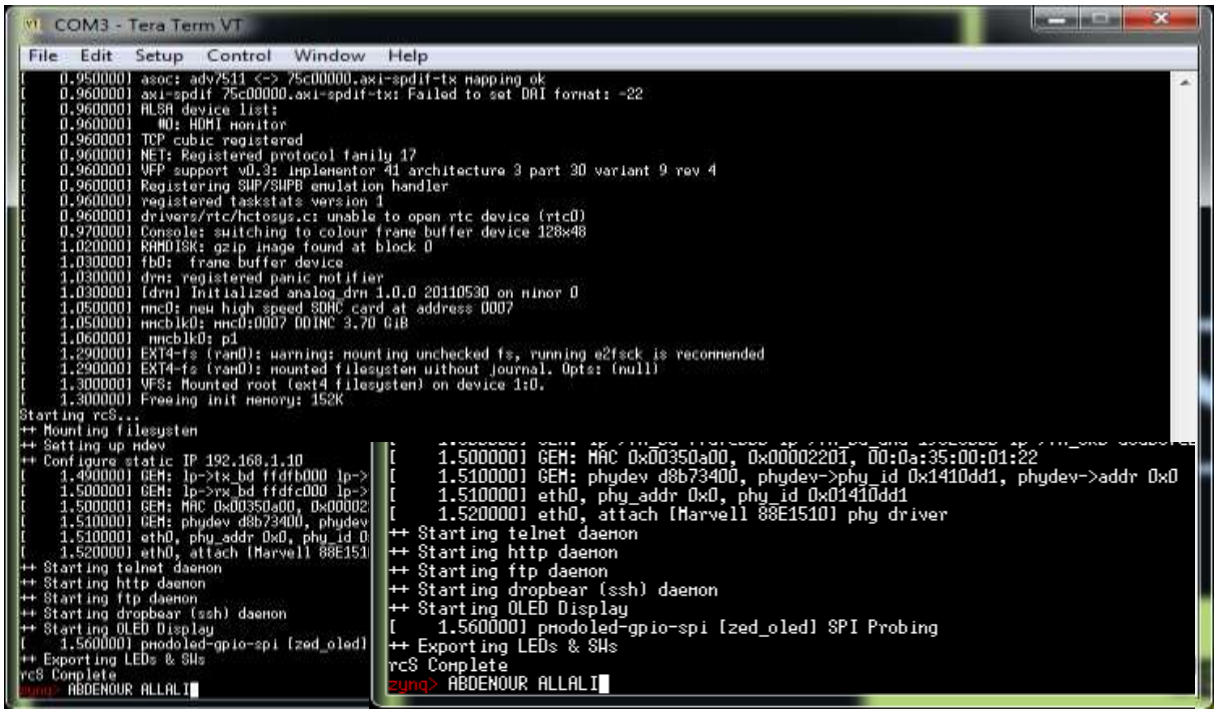

Figure 4.22 Linux Command Prompt Following Boot

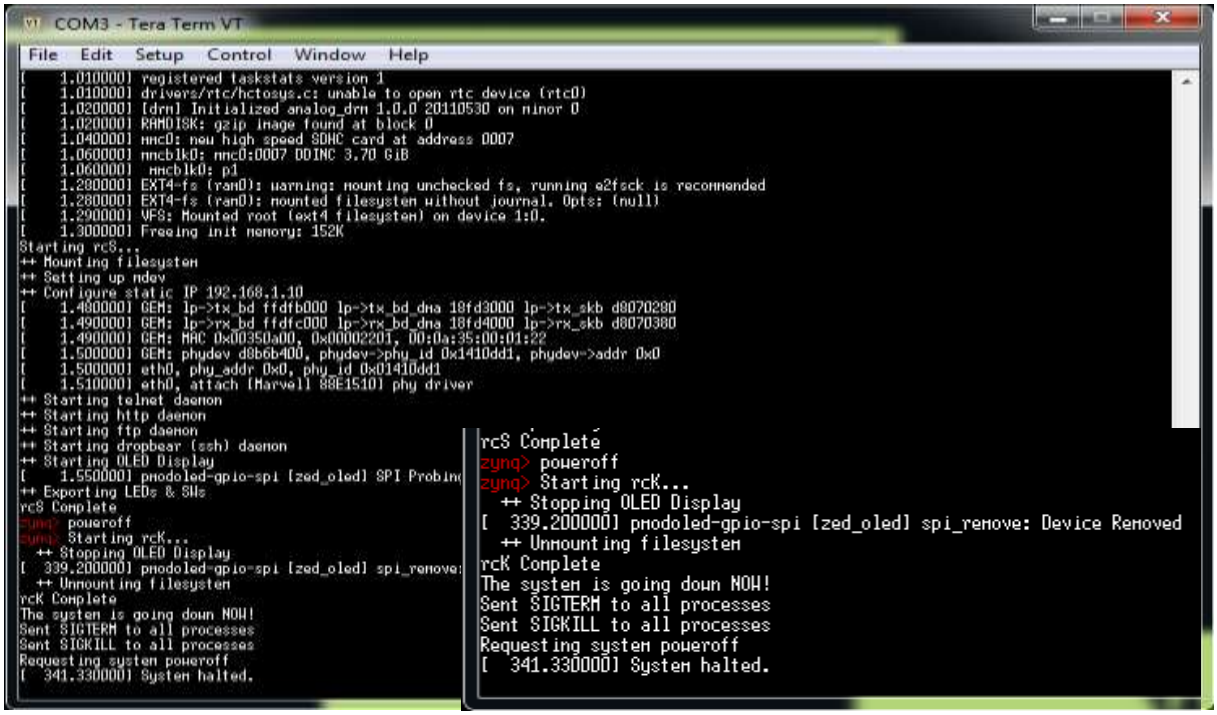

Figure 4.23Linux Command Prompt Following Shutdown

4.8 FPGA implementation with MATLAB System Generator configuration

In this section, we presented how the hardware implementation was performed. First, we started with the Xilinx System Generator (XSG) design, followed by testing and validating the designed architecture on FPGA from MATLAB Simulink (hardware co-simulation). Finally, weended up testing the implementation in real-time.

We aim to provide hardware architecture for ECG signal filtrations. The best choices to carry out this architecture are the FPGA devices, which combine the high performance of ECG signal de-noising. The implementation has been designed using Xilinx System Generator and the Zed Board evaluation Kit.

The XSG is a high-level tool that uses MATLAB Simulink environment to create and verify Xilinx FPGA design quickly and easily. It provides a library of bits and cyclesin accurate floating-point and fixed-point implementations.

Moreover, the cascaded FIR filter block can build high performance in Simulink using the Xilinx Block set, which contains functions for signal processing, error correction, arithmetic, memories and digital logic.

The Xilinx System Generator includes a code generator that automatically generates a synthesized VHDL code from the created model, which can be implemented in the FPGA [209]. Figure 4.24 describes the top-level diagram of the suggested architecture, and it consists of three main subsystems: high pass filter block, band stop filter block and low pass filter block. Moreover, a block to download the ECG signals from MATLAB, a gateway in/out to pass from floating-point MATLAB to FPGA fixed point and a display to show the appropriate classes of the cascaded filter block. In the following, we describe in detail the main parts of each section. In the filters blocks, the FDA Tool levels are implemented on FPGA using a pair of low pass, band stop and high pass filters corresponding to the high, medium and low frequency, respectively. Figure 4.25 describes the top-level diagram of the cascaded FIR filter. Using the (H-B-L) configuration with the Rectangular window, the hardware implementation of the ECG signal de-noising filters has been achieved.

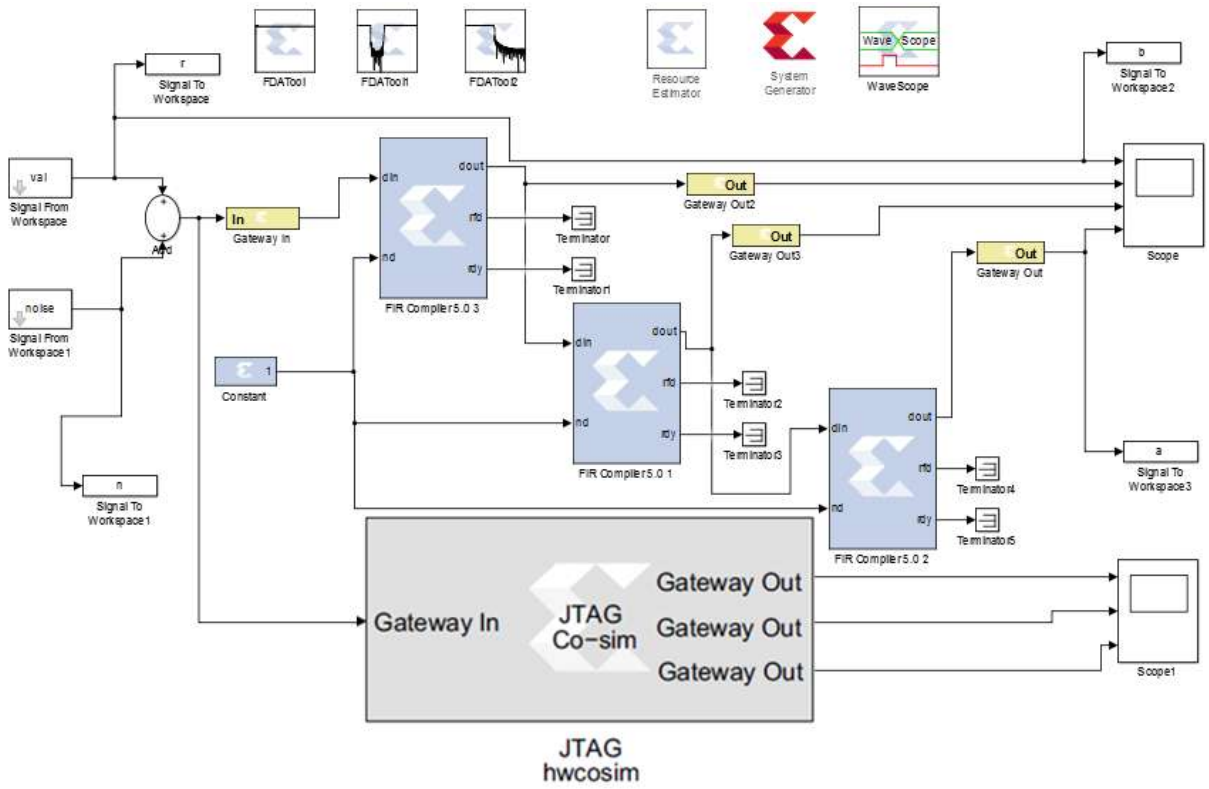

Figure 4.24 Hardware Co-simulation model of Designed Filter

After the successful simulation using XSG block sets, the designed architecture is ready to be transferred to the FPGA board. The XSG can be executed on FPGA from MATLAB, using the hardware co-simulation offered by the System Generator block; the compiled model is transferred directly from MATLAB Simulink to the FPGA board. The compilation automatically creates the bit stream and compiles the JTAG block. When the compilation is in progress, the data are transferred simultaneously between the computer and the board. Therefore, it is possible to read the filter outputs from JTAG and display them in Simulink.

4.8.1 Hardware Co-Simulation Features

The design of the filter with Rectangular Window and cascaded FIR filter technique is carried out. The implementation on FPGA Zync x7z020-3clg484 target device is achieved, the order of each filter method is used as 360, and the results of filter implementation using the Rectangular window method are as follows.

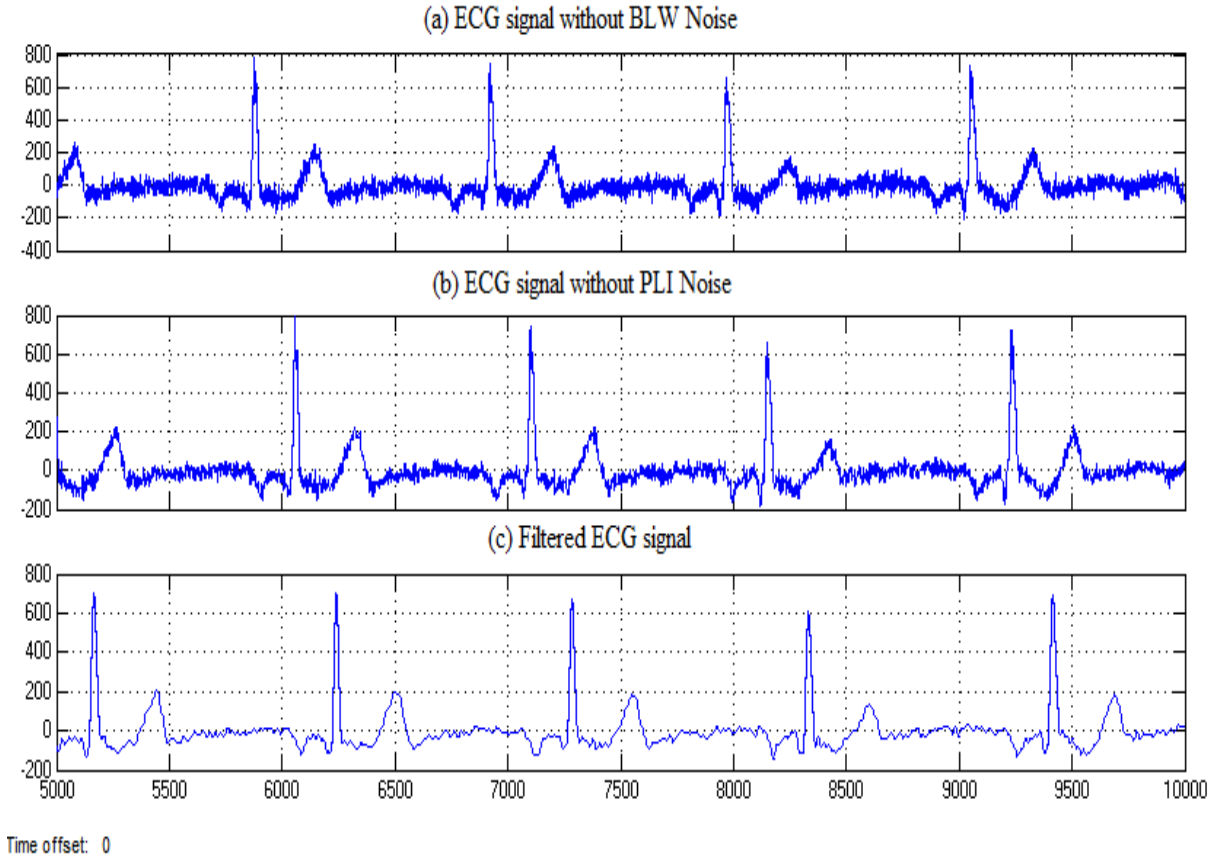

Figure 4.25Hardware co-simulation results of Filtered ECG signal of the cascaded FIR filter Design

The contribution that we have made in the field of Hardware co-simulation has achieved remarkable success by comparing the signals that were monitored from the output of the Zed board and the signals resulting from the simulation system. Clearly, we find that the results given by the FPGA implementation are purer while achieving the desired goal, which is to preserve the data ECG signal Task with real-time response.

The resource usage reports for FPGA implementation using the ISE design suit 14.5 show that this contribution has been very successful in terms of containing a small number of chips, reducing the usage of Flip Flops and defining the number used for LUTs, see Figure 4.26 meaning that embedding can bring better advantages in the SoC field It is less expensive and faster to implement.

cw Project Status (12:02:36)			
Project File:	cw.ise	Current State:	Synthesize
Module Name:	cw	• Errors:	No Errors
Target Device:	Zynq xc7z020-3clg484	• Warnings:	851 Warnings
Product Version:	ISE 14.5 WebPACK	• Routing Results:	
Design Goal:	Balanced	• Timing Constraints:	
Design Strategy:	Xilinx Default (unlocked)	• Final Timing Score:	

cw Partition Summary	[-]
No partition information was found.	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	Used	Available	Utilization
Number of Slices	3491	3992	99%
Number of Slice Flip Flops	7284	9214	89%
Number of input LUTs	4763	9214	61%
Number of bonded IOBs	18	189	3%
Number of GCLKs	1	18	3%

Figure 4.26 Resource utilization report of cascaded FIR filter design using ISE Design suit 14.5

4.9 Conclusion and Future direction work

In this chapter, we have proposed to tow alternative methods for building a cascaded FIR filter to enhance the ECG signal quality, according to high measurements of SNR and low MSE. In the first algorithm, the cascaded FIR filter is released by selecting the type of

windows. In the second algorithm, the cascaded FIR filter is removed by adopting the position of the FIR filters. In both cases, we find that the rectangular window is more effective than the others. Then the configuration (H-B-L) achieves remarkable success in improving the quality of the ECG signal.

A real-time implementation of the ECG signal filtering system is achieved. The plan was successfully implemented on ZedBoard FPGA. Then, we developed an optimized software algorithm that can best ECG signal de-noising into normal and abnormal and using noisy ECG signals. The method requires a minimum number of statistical features, optimizing memory space requirements. Then, this method was implemented in a real-time FPGA-based system to provide a system that can help patients and doctors with heart disease monitoring and diagnosis.

The present work demonstrates the reduction of ECG noise by addressing some challenging issues. However, there are still some open issues to be implemented in the future, including the following.

In this chapter, we have mentioned embedded system extensions using FPGAs, and they are currently in the process of publishing this topic as a journal article.

Research is ongoing for the idea of developing technology similar to a pacemaker, which in turn helps support cardiac performance in ischemic heart patients.

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Conclusion

This thesis contains a comprehensive study of the ECG signal, as it includes several interrelated chapters containing a series of information about the human heart in terms of organic surgery for it and the basics of selecting the ECG signal, as well as a historical brief on discovering the importance of this signal in clinical care for patients And mechanisms for invention and monitoring devices, as we have covered comprehensively about signal processing with its accompanying technologies. We have also given the possibility of a significant extension to talk about SoC technologies and contribute to implementing embedded systems. Similarly, to our work, which is not limited to what we mentioned previously, but came as a result of two articles that have been published In two different magazines as these two articles contained two other methods for filtering the ECG signal from the impurities that it encounters during and after monitoring it from the heart. The idea generally revolves around using a cascaded filter with three floors from FIR filters. i.e. Usinga cascaded filter configured by three FIR filters, the first method involves studying the purification of the ECG signal by selecting the windows combined with the cascaded filter parts. The second method consists in analyzing the filtering of the ECG signal by analyzing the variance resulting from the exchange of the positions of the filters that form the cascaded filter. Both methods brought impressive results in comparison with previous recent works. Thus, we concluded that these two methods gave equivalent results, regardless of the method applied. We add to this work a fundamental result in the field of ECG signal processing: the two methods provide the same target, and we conclude that they enable us to apply them to other signals relatively similar to the ECG signal. We have also offered an extension to contribute to the inclusion of FPGA by harnessing Matlab Simulink SG, connected with XILINX ZedBoard, where the magnificence of this contribution has received remarkable results that are of great importance in the field of embedded systems.