وزارة التعليـــم العالـــي و البحث العلمـــي

Ministère de l'Enseignement Supérieure et de la Recherche Scientifique

جامعة فرحـات عبـاس سطيـف

UNIVERSITE FERHAT ABBES – SETIF
UFA (ALGERIE)

MEMOIRE

PRESENTE AU DEPARTEMENT D'ELECTROTECHNIQUE

FACULTE DE TECHNOLOGIE

Pour obtenir le titre de

MAGISTER EN ELECTROTECHNIQUE

OPTION: Machines Electriques Et Leurs Commandes

Par

CHIHI ABLA

Thème

Power Factor Correction Of Single Phase AC-DC Converter

Soutenu le : 27 /10 /2010 devant le jury composé de:

Pr. MOSTEFAI	MOHAMED	Université Ferhat Abbes-Setif-	Président
Dr. RAHMANI	LAZHAR	Université Ferhat Abbes-Setif-	Encadreur
Dr .RADJEAI	HAMMOUD	Université Ferhat Abbes-Setif-	Examinateur
Dr. HEMSAS	KAMEL EDDINE	Université Ferhat Abbes-Setif-	Examinateur

DEDICATION

I dedicate this memory to:

My very dear parents

My darling husband

My very lovely girl

My brothers and sisters

And all my friends

ACKNOWLEDGMENTS

I would like to express my sincere appreciation to my advisor, Dr. Rahmani, for his guidance, encouragement, and continued support throughout the course of this work. His extensive knowledge, advice and creative thinking have been an invaluable help to this work.

That all professors who contributed to my formation; find in this modest work the testimony of my deep and sincere gratitude.

I would like to thank my husband, for his support, and understanding during the past years.

To all those that contributed from far or meadows, to the implementation of this job, address my alive acknowledgments.

That the set of jury is thanked to have accepted judge my work.

SUMMARY

CHAPTER 3 : **Fuzzy Logic Control For Active Power Factor Correction**

ABSTRACT.

This study presents the analysis, a modeling approach to obtain a small-signal model, design and the Matlab/Similink implementation of a linear control technique for single-phase boost power factor correctors (PFC). Such converters present nonlinear characteristics and an approximation of them are used to drive the models. The most important result obtained is that the small-signal output is not equal to the load impedance. The proposed circuit significantly improves the dynamic response of the converter to load steps without the need of a high crossover frequency of the voltage loop by adding low-pass filter, so that a low distortion of the input current is easily achieved in PI-PI Control for Active Power Factor Correction. After that, a modeling approach to obtain a small-signal model and the simulation of a PI controller in the loop voltage and two controllers in the loop current based on a standard fixed and sinusoidal band hysteresis control, followed by a variable band hysteresis control for a single-phase power factor corrector (PFC). Finally, a fuzzy logic controller in the loop voltage and hysteresis controller in the loop current for a single-phase power factor corrector (PFC).

Key words: *Power Factor, Rectifier, AC-DC, Correction, PI, Hysteresis, Fuzzy*

RESUME.

Cette étude présente l'analyse, une approche de modélisation pour obtenir un modèle de signal unique, la conception et l'implémentation sous Matlab/Similink d'une technique de contrôle linéaire pour les correcteurs du facteur du puissance monophasés (PFC). Tels convertisseurs présentent des caractéristiques nonlinéaires et une approximation d'eux sont utilisées pour conduire les modèles. Le résultat le plus important obtenu est que la production d'un signal de sortie unique n'est pas égale à l'impédance de la charge. Le circuit proposé améliore considérablement la réponse dynamique du convertisseur pour les pas de la charge sans le besoin d'une haute fréquence de la boucle de tension en ajoutant un filtre passe - bas, afin qu'une basse distorsion du courant d'entrée soit atteindre facilement dans la commande PI-PI Pour la correction du facteur de puissance. Après cela, une approche de modélisation aussi pour obtenir un modèle de signal unique et la simulation d'un contrôleur PI dans la boucle de tension et deux contrôleurs dans la boucle du courant basé sur la commande hystérésis à bande fixe et à bande sinusoïdale, suivi par la commande hystérésis à bande variable et finalement, un contrôleur de la logique flou dans la boucle de tension et un contrôleur hystérésis dans la boucle du courant pour la correction du facteur de puissance (PFC) en monophasé.

Mots clés : *Facteur de puissance, redresseurs, AC-DC, Correction, PI, Hystérésis, floue*

ملـــخص.

هذه الدراسة قدمت لنا تحليلا، ونهج النمذجة للحصول على نموذج صغير إشارة وتصميم وتنفيذ برنامج مطلب /سيميلنك لتقنية التحكم الخطية لمصححات عامل الاستطاعة أحادية الطور. مثل هذه المحولات تقدم صفات غير خطية و حسابها يستعمل لقيادة النماذج الالكترونية. النتيجة المهمة المتحصل عليها أن إنتاج إشارة خروج وحيدة لا تساوي ممانعة الحمولة. الدارة المقترحة تحسن بكثرة الاستجابة الديناميكية للمحول لآجل خطوات الحمولة بدون الحاجة إلى تردد عالي لحلقة التوتر بإضافة مصفاة عبور منخفض للتوصل إلى انحراف منخفض لتيار الدخول بسهولة في التحكم PI-PI لتصحيح عامل الاستطاعة . بعد ذلك ، التركيب للحصول على نموذج وحيد الإشارة و تصنيع مراقب PI في حلقة التوتر و مراقبين في حلقة التيار مؤسس على التحكم التراجعي ذو شريط ثابت وآخر ذو شريط تموجي جيبي ، يتبع بالتحكم التراجعي ذو شريط متغير ، أخيرا ، استعمال مراقب المنطق الضبابي في حلقة التوتر والمراقب التراجعي في حلقة التيار لتصليح معامل الاستطاعة (PFC) في النظام أحادي الطور.

الكلمات المفتاحية : *تصحيح, PFC, PI, المحولات AC/DC*

INTRODUCTION.

Most electronic equipment is supplied by 50 Hz utility power, and more than 50% of this power is processed through some kind of power converter. Usually power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. Since these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage, the input line current contains rich harmonics, which pollute the power system and interfere with other electric equipment. These converters usually have a low power factor.

When a converter has less than unity power factor, it means that the converter absorbs apparent power higher than the real power it consumes. This implies that the power source should be rated with higher VA ratings than the load needs. In addition, the current harmonics the converter produces deteriorate the power source quality, which eventually affect the other equipment. The simple solution to improve the power factor is to add a PFC to achieve a good power factor. called a PFC stage, is usually inserted in the equipment to shape the line input current into a sinusoidal waveform and its line current is in phase with the line voltage.

Among three basic power converter topologies (boost, buck and buck-boost), the boost converter is shown is the one most suitable for power factor correction applications. This is because the inductor is in series with the line input terminal through the diode rectifier, which gives lower line current ripple and continuous input current, the buck converter is seldom used as a power factor correction application, since the input current is discontinuous and it loses control when the line input voltage is lower than the output voltage. The buck-boost and flyback converters are able to control the average line input current. However, the power handling capability is smaller because of its higher voltage and current stresses. Therefore, the boost converter is currently the most popular PFC topology. To achieve unity power factor, the input power is the squared sine waveform while the output power is usually constant for most applications [1].

To meet the IEC requirements, a PFC circuit should be added in the system. A frequently used boost PFC circuit can be inserted into the system. However, after adding the PFC function, the cost of the system will increase and the efficiency of the system will decrease. [2]; a big number of the power factor correctors of AC/DC converters has been proposed in the literature, some practical works of simulation under Simulink (simulator of dynamic

systems under Matlab), will permit to validate the study, to examine rapidly different command modes of this converter, to observe unique or with difficulty measurable signals,

Commonly, a linear controller (PI-PI controller) is designed utilizing a small-signal model that is obtained by linearization about an operating point [3] in both, outer loop for output dc voltage regulation (loop voltage) and inner loop so that the line current is sinusoidal and in phase with the line voltage (loop current). The system provides acceptable performance. In [4], a PI control scheme is presented that includes a 100 Hz notch filter in the voltage control loop. The notch filter reduces the amount of second harmonic that is reaching the multiplier. Thus, the voltage loop bandwidth can be increased, which leads to a faster transient response, without the penalty of increased third harmonic in line current in steady state. The improvement in the transient response of the loop voltage controller degrades the quality of the input current (High THD). On the other hand, PI controller design in loop current requires an accurate mathematical model of the plant and it failed to perform satisfactorily under parameter variation, nonlinearity (two multiplications), load disturbance, etc [5]. Hysteresis current controller (bang-bang hysteresis (BBH) technique) has an advantage in coping with the time varying nonlinearity of switches in PFC pre-regulator, and it does not require an accurate mathematical model of the PFC pre-regulator when the controller is being designed [6]. Also this technique has an advantage of yielding instantaneous current control [7], which results in very fast response and increased 'boost' switch reliability. However, it has a serious disadvantage in that the switching frequency of the boost switch f_{sw} is not constant and varies in a wide range during each half cycle of the ac input voltage[8], [9]. The switching frequency is also sensitive to circuit component values, design parameters and difficult for EMI filter design. The novel feature of the proposed method resides in the fact that unity power factor and nearly sinusoidal inputs current are obtained at constant switching frequencies [10], [11]. Moreover, the method exhibits instantaneous current control, which results in very fast response and increased switch reliability.

The fuzzy approach also, offers the possibility to model a non–linear system on the basis of the knowledge of many non-well defined relations among the variables of the system, and to design a controller that adapts itself to several working conditions.

Thus, fuzzy logic seems a suitable solution both to model and to control power electronic systems [12].

PI-PI Control for Active Power Factor Correction in chapter 1 presents a systematic analysis, a modeling approach to obtain a small-signal model, design and digital implementation of the

standard cascaded linear controller along with using a 100 Hz notch filter in a voltage loop of a regulated dc voltage. This controller is verified by detailed MATLAB/Simulink based simulations through the use of a continuous time plant model and a discrete time controller.

Chapter 2 covers a systematic design, and simulation comparison, PI controller for a voltage loop of a regulated dc voltage, standard hysteresis controller and redesign of the standard hysteresis controller with some modifications for improved performance for a current loop. All these controllers are verified by detailed MATLAB/Simulink based simulations using a continuous time plant model and a discrete time controller. These controllers are compared for steady-state performance and transient response over the entire range of input and load conditions for which the system is designed.

In Chapter 3; Fuzzy Logic Control for Active Power Factor Correction is proposed; in this case, PI controller will be replaced by fuzzy logic controller for a voltage loop of a regulated dc voltage; and standard hysteresis controller for a current loop. These controllers are verified by detailed MATLAB/Simulink based simulations using a continuous time plant model and a discrete time controller and are compared for steady-state performance and transient response.

REFERENCES.

[1]. Jinrong Qian. **"Advanced Single-Stage Power Factor Correction Techniques".** Dissertation submitted to the faulty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering**.** September 25, 1997

[2]. Yiqing Zhao. "**Single Phase Power Factor Correction Circuit with Wide Output Voltage Range".** Thesis submitted to the Faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of Master of Science In Electrical Engineering. February 6, 1998

[3]. Zaohong Yang and Paresh C. Sen. **"A Novel Technique to Achieve Unity Power Factor and Fact Transient Response In Ac-to-Dc Converters**," IEEE Transaction on Power Electronics, vol. 16, no. 6, pp. 764–78, Novembre 2001.

[4]. L.Rahmani, F.Krim, A.Bouafia. **"Deadbeat Control for PWM AC Chopper,**" Taylor & Francis, Electric Power Components and systems, 32:453-466, 2004.

[5]. L.Rahmani, F.Krim, M.S.Khanniche, A.Bouafia. "**Control for PWM AC Chopper feeding nonlinear loads,"** Taylor & Francis, INT. J. ELECTRONICS, Vol 91, No 3, March 2004, 149-163.

[6]. Diego G. Lamar, Arturo Fernandez, Manuel Arias. "**A Unity Power Factor Correction Preregulator With Fast Dynamic Response Based on a Low-Cost Microcontroller,"** IEEE Transaction on Power Electronics, vol. 23, no. 2, pp. 635–641, March 2008.

[7]. Martin K. H. Cheung, Martin H. L. Chow, Chi K. Tse. **"Practical Design And Evaluation of A 1 KW PFC Power Supply Based en Reduced Redundant Power Processing Principle**," IEEE Transaction on Industrial Electronics, vol. 55, no. 2, pp. 665–673, February 2008.

[8]. Vishnu Murahari Rao, Amit Kumar Jain, Kishore K. Reddy and Aman Behal. **"Experimental Comparison of Digital Implementation of Single-Phase PFC Controllers**," IEEE Transaction on Industrial Electronics, vol. 55, no. 1, pp. 67–78, January 2008.

[9]. John Chi Wo Lam and Praveen K Jain. "**A Modified Valley Fill Electronic Ballast Having a Current Source Resonant Inverter With Improved Line- Current Total Harmonic Distortion (THD), High Power Factor, and Low Lamp Crest Factor**," IEEE Transaction on Industrial Electronics, vol. 55, no. 3, pp. 1147–1159, March 2008.

[10]. N. Belhouchet and L.Rahmani. **"Development of Adaptative Hysteresis-band Current Control of PWM Three-Phase AC Chopper with Constant Switching Frequency,**" Taylor & Francis, Electric Power Components and systems, 37:583-598, 2009.

[11]. N. Belhouchet, L.Rahmani and S. Begag. **"A novel adaptative HBCC technique for three-phase shunt APF,**" Elsevier, Electric Power Systems Research, 79, 2009, 1097-1104.

[12]. Simon Wall and Robin Jackson**. "Fast Controller Design for Single-Phase Power-Factor Correction Systems**," IEEE Transaction on Industrial Electronics, vol. 44, no. 5, pp. 654–660, October 1997.

CHAPTER 1

PI-PI CONTROL FOR ACTIVE POWER

FACTOR CORRECTION

Abstract**—***this chapter presents the analysis, a modeling approach to obtain a small-signal model, design and the Mathlab/Similink implementation of a linear control technique for single-phase boost power factor correctors (PFC). Such converters present nonlinear characteristics and an approximation of them are used to drive the models. The most important result obtained is that the small-signal output is not equal to the load impedance. The proposed circuit significantly improves the dynamic response of the converter to load steps without the need of a high crossover frequency of the voltage loop by adding low-pass filter, so that a low distortion of the input current is easily achieved. This controller has been verified via simulation in Simulink using a continuous time plant model and a discrete time controller.*

1.1. INTRODUCTION.

Single-phase power factor correction (PFC) circuits provide rectification of the line voltage to a regulated dc voltage while shaping the input current to be a sinusoid and in phase with the line voltage [1]. Often, the PFC acts as a preregulator to a dc–dc converter that may be used to provide additional regulation and ohmic isolation [2], [3]. Due to adoption of IEC 1000-3-2 [4] as the EN61000-3-2 norm in Europe and the formulation of the IEEE 519 [5] in the USA, these circuits are increasingly being used in the front-end of electronic equipment. Among the several possible topologies [2], the boost PFC shown in Fig. 1.3 is most commonly used. The control objectives are to track the inductor current to a rectified Sinusoid (so that the line current is sinusoidal and in phase with the line voltage) and to regulate the average output voltage to a desired magnitude and to has a fast response to the load variation [6], [7].

Commonly, a linear controller is designed utilizing a small-signal model that is obtained by linearization about an operating point [6]. The system provides acceptable performance. However, the controller has an inherent drawback of third harmonic in the input current. This happens because the reference current signal is the product of an output voltage error amplifier (that contains a second-harmonic component) and the input voltage wave shape. Thus, the voltage loop gain at 100 Hz effectively determines the level of third harmonic to be expected in the input voltage [8]. Several commercial ICs incorporate the required analog components to implement the linear control scheme. Recently, there has been a significant interest in an all-digital implementation, available

for the PFC application, digital implementation of the linear control design using commercial microcontrollers and DSPs has been carried out. Since the computation time of commercial low-cost microcontroller is significantly high, a discrete version of the conventional analog design cannot be directly implemented without significant modification to the design of the voltage control loop. To improve the dynamic response of the converter to load steps, the 100 Hz notch filter is inserted to the voltage control loop. The notch filter reduces the amount of second harmonic (to cancel the output voltage ripple) that is reaching the multiplier. Thus, the voltage loop bandwidth can be increased, which leads to a faster transient response, without the penalty of increased third harmonic in steady state. For faster dynamic response, current mode control is adopted instead of voltage mode control. Both peak current mode and average current mode controls are widely used [9]. The main deference between the two methods is that, in the later, the sensed inductor current signal is averaged and compensated by a current compensation network [10], while in the former; only inductor current is sensed and used [11]-[12]. Although noise in average current mode control can be suppressed, the architecture of the system with average current mode control is complicated. Therefore, peak current mode control is used, and an optimal proportional integral (PI) controller designed by utilizing a small-signal model is adopted to achieve fast dynamic response, simplicity, and easy implementation. This chapter presents a systematic analysis, a modeling approach to obtain a small-signal model, design and digital implementation of the standard cascaded linear controller along with using a 100 Hz notch filter in a voltage loop of a regulated dc voltage. This controller is verified by detailed MATLAB/Simulink based simulations through the use of a continuous time plant model and a discrete time controller.

1.2. CLASSIC CONVERTER.

Fig. 1.1 represents the solution commonly adopted for the conversion in single phase AC-DC. It is about a full bridge of four diodes rectifier feeding a RC load.

Fig. 1.2 represents the simulation waveforms of DC-Bus voltage, of the input current and its spectrum. The input current is much distorted due to large discontinuities with THD of 69.77%

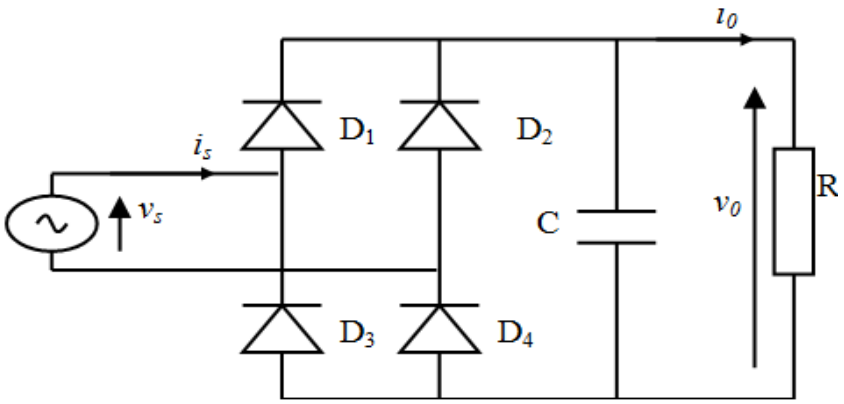

Fig. 1.1. Full Bridge Rectifier.

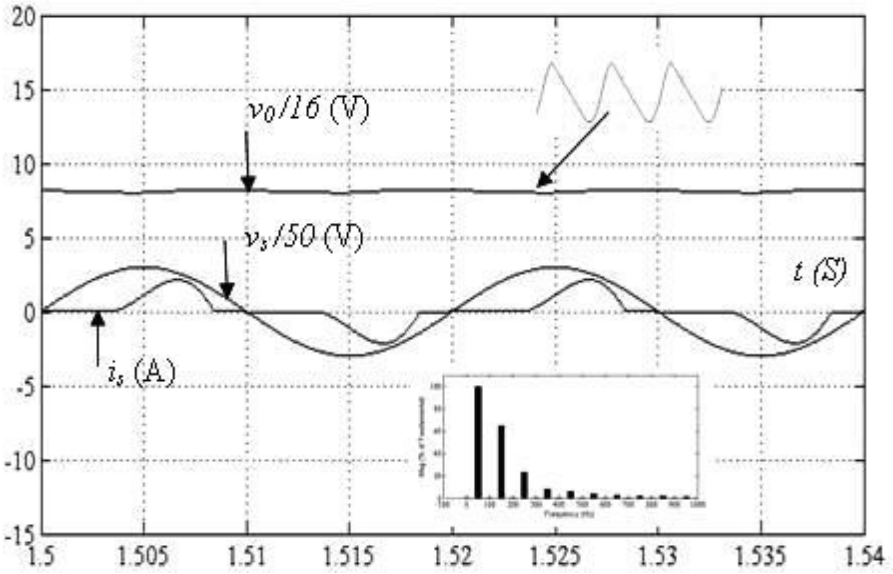

Fig.1.2. The input current and DC-Bus Voltage

R=212 Ω, C=940 μF, L= 37.3 mH, V_{SM}=150 V.

As we observe in Fig. 1.2 the deformation in the shape of the input current, therefore, the power factor at the input side is variable and weak in some cases because of the raised harmonic distortion of the current wave.

To limit the ominous effects of the LF disruptions, the norm IEC 61000-3-2 governs, the harmonic of the current absorbed by the network for currents not exceeding 16A by phase is about 3,7 KVA in single phase. Therefore, it is necessary to put to the point of the solutions permitting to reduce the LF disruptions of AC-DC classic converter. These solutions, regrouped under the name (Power Factor Correction or PFC), must permit to

absorb on the network a current the more sinusoidal possible with a minimum of phase angle between the fundamental of the current absorbed and the input voltage.

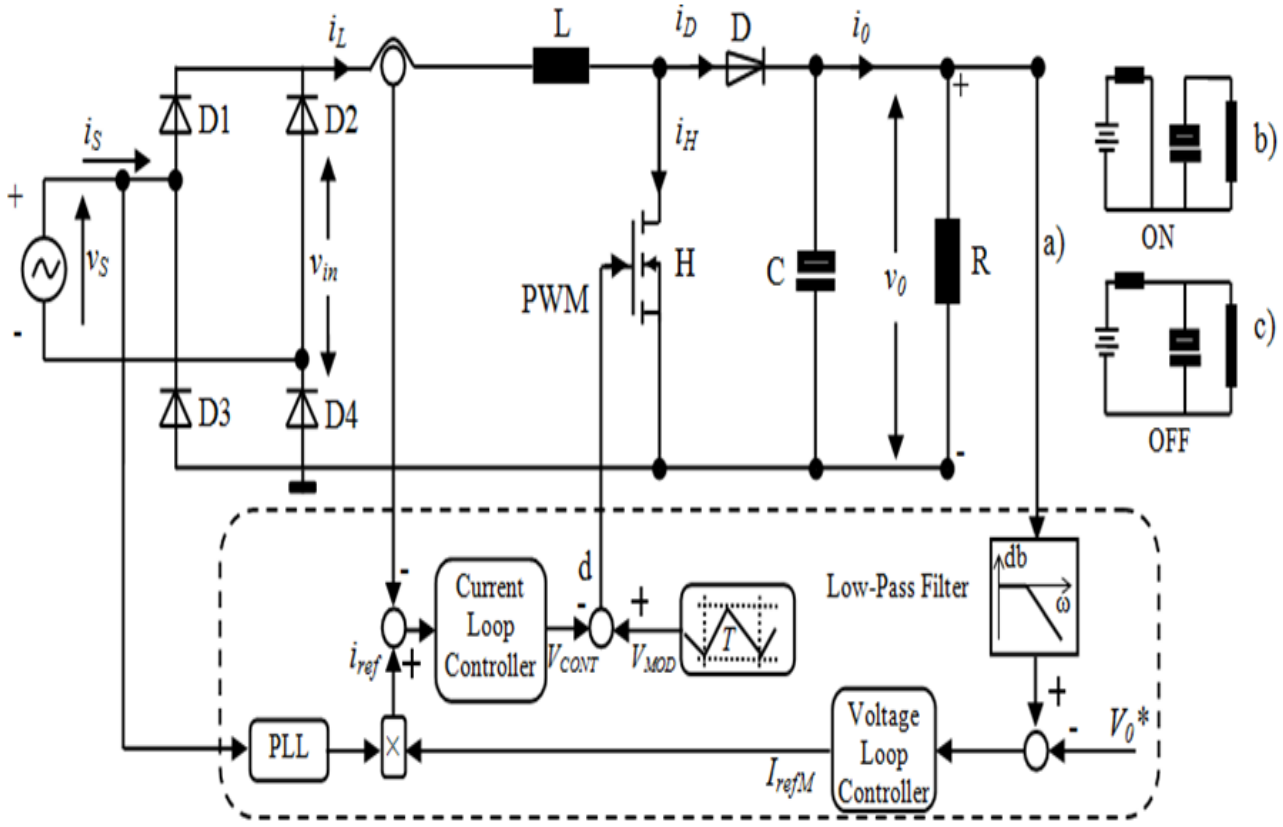

Fig.1.3. PFC preregulator.

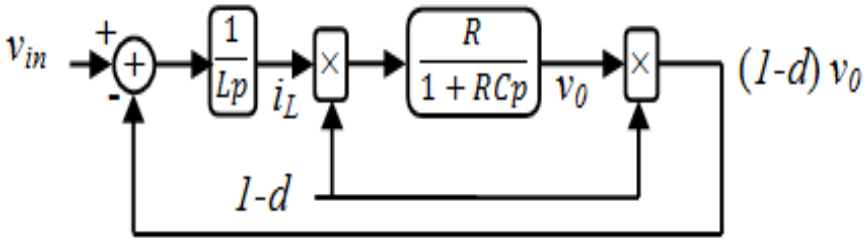

Fig.1.4. Block diagram of the PFC preregulator.

1.3. PRINCIPALS OF OPERATION.

The basic circuit diagram of the dc/dc converter with front–end solid-state input power factor conditioner used in the proposed scheme is shown in Fig.1.3a and Fig.1.4.

The power circuit is that of an elementary step-up converter. When the boost switch *H* is turned on (*d=1*) Fig.1.3b, the inductor current builds up, and energy is stored in the

magnetic field of the inductor, whereas the boost diode *D* is reverse biased, and the capacitor supplies power to the load. This is the first mode operation. As soon as the boost switch is turned off (*d=0*) Fig.1.3c, the power circuit changes mode, and the stored energy in the inductor, together with the energy coming from the input ac source, is pumped to the output circuitry (capacitor-load combination). This is mode 2 of the circuit. Then the state space model for the boost PFCS in continuous current mode can be found by the circuit analysis of fig.1a. The output voltage and inductor current dynamics are governed by the variable structure real switched system equations (1.1).

$$\begin{cases} \dfrac{dv_0}{dt} = \dfrac{1}{C}[(1-d)i_L - (1/R)v_0] \\ \dfrac{di_L}{dt} = \dfrac{1}{L}[v_{in} - (1-d)v_0] \end{cases} \tag{1.1}$$

In order to obtain a sinusoidal input current in phase with the input voltage, the control unit should act in such a way that v_{in} sees a resistive load equal to the ratio of v_{in} and i_L. This has been done by comparing the actual current passing through the inductor with a current reference, which is derived from v_{in} and has amplitude determined by the output voltage controller.

Since the break frequency of the output filter is very low, one can say that the output voltage is controlled only by the average value of the on-duty ratio of the switch in half cycle of the ac input voltage α:

$$V_0 = \frac{V_{in,ave}}{1-\alpha} = \frac{2}{\pi} V_{SM} \frac{1}{1-\alpha} \tag{1.2}$$

Where

d : Logical variable to represent the state of the boost switch,

$V_{in,ave}$: average value of the full-wave rectified sinusoidal input voltage,

V_{SM} : Peak value of the sinusoidal input voltage.

1.4. STATIC ANALYSIS OF POWER FACTOR CORRECTOR PREREGULATORS WITH FAST DYNAMICS.

The control by current imposes the average power

$$P = \frac{1}{T/2}\int_0^{T/2} |v_S(t)||i_0(t)|dt = \frac{1}{T/2}\int_0^{T/2} |V_{SM} sin\omega t|\,\left|I_{refDC}\, sin\omega t\right| dt = \frac{V_{SM} I_{refDC}}{2} \quad (1.3)$$

passed to the load with the ideal PFC preregulators. This behavior in generator of power lets free the voltage v_S to progress according the load R in the report v_S^2/R. Generally, the users ask for generators of voltage. It follows the necessity of an automatic adaptation of the power supplied to the load according to its variations to maintain v_s. Fig.1.3a shows the voltage loop v_s of which the gating control signal will act on the amplitude of the reference current with a constraint of sinusoidal shape.

A low-pass filter is included in the output voltage feedback loop to eliminate *100 Hz* output voltage ripple Fig.1.5. The output of the voltage feedback loop is therefore a *DC* value I_{refDC}. The input line current reference is therefore a sinusoidal waveform and the input line current $i_S(t)$ (assuming the current loop to be ideal) has no distortion.

$$i_S(t) = \frac{V_{SM}|\sin(\omega t)|I_{refDC}}{K_s} \quad (1.4)$$

PFC preregulators have a high efficiency (around 95%). So

$$v_S(t) i_S(t) = V_{0DC} i_0(t) \quad (1.5)$$

Moreover, the output capacitor *C* is big enough to keep the output voltage to his *DC* component V_{0DC}. So

$$i_0(t) = \frac{V_{SM}^2 I_{refDC}}{2K_s V_{0DC}}[1 - \cos(2\omega t)] \quad (1.6)$$

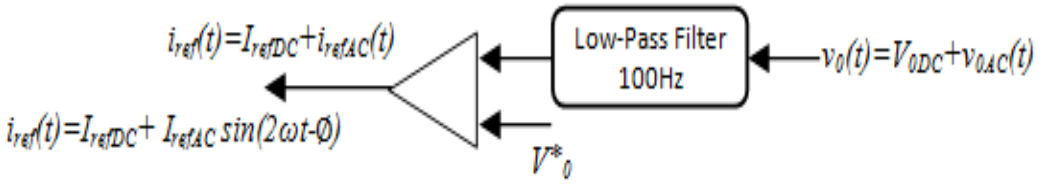

Fig. 1.5. Voltage Loop.

As can be seen in Fig.1.5 and in (1.6), the output current has a *DC* Value and a second harmonic. This second harmonic is processed through the bulk capacitor. A voltage ripple thus appears at the output voltage and is transmitted into the output voltage feedback loop. For this reason, a low-pass filter is needed in order to attenuate and quasi- eliminate this distortion and keep the input line current sinusoidal, as can be seen in (1.4). However, the low-pass filter decreases the feedback bandwidth of the output voltage, causing a poor dynamic response of the output voltage in PFC preregulators. This chapter will next consider the situation in which the corner frequency of the low-pass filter (f_{CV}) place in the output voltage feedback is increased in order to improve the response of the output voltage in PFC preregulators. The PFC preregulator's priorities change: the main objective is to improve the output response instead of drawing a sinusoidal input current to obtain PFC preregulators with fast dynamics. The output voltage ripple of double line frequency is transferred into the output voltage feedback loop. Thus, the output of the voltage feedback loop (i_{ref} is not a constant value).

$$i_{ref}\,(t) = I_{refDC} + I_{refAC}\sin(2\omega t - \emptyset) \tag{1.7}$$

Where I_{refAC} is the second harmonic amplitude of i_{ref} and Ø is the phase lag with respect to $|v_s(t)|$ of the second harmonic of i_{ref}.

From Fig.1.5 and by replacing the value of I_{refDC} for $i_{ref}(t)$ in (1.4)

$$i_S(t) = \frac{V_{SM}}{K_s}\left[I_{refDC}\,\sin(\omega t) + \frac{I_{refAC}}{2}\cos(\omega t - \emptyset) - \frac{I_{refAC}}{2}\cos(3\omega t - \emptyset)\right] \tag{1.8}$$

The input current, therefore, is not sinusoidal. The second harmonic of $i_{ref}(t)$ is transformed into the third harmonic of the input line current. Furthermore, input line current distortion is defined by the ripple characteristics of the output of the voltage

feedback loop (I_{refAC} and Ø)

Substituting (1.8) in (1.5) and supposing an output bulk capacitor big enough to keep the output voltage constant, the output current is

$$i_0(t) = I_0 + i_{02}(t) + i_{04}(t) \tag{1.9}$$

Moreover, K_S can be easily calculated as a function of averaged power processed by the PFC preregulator from I_0 in (1.9)

The average power processed to the load become

$$P = \frac{V_{SM}^2}{2K_s}(I_{refDC} + \frac{I_{refAC}}{2} sin\emptyset) \tag{1.10}$$

Then

$$K_s = \frac{V_{SM}^2}{2P}(I_{refDC} + \frac{I_{refAC}}{2} sin\emptyset) \tag{1.11}$$

If the ripple of the output feedback loop I_{refAC} and the phase leg Ø are assumed to be equal *0* and replacing *P* obtained from (1.3) in (1.11), the expressions of *P* and K_S become: $P=(V_{SM}\, I_{refDC})/2$, $K_S=V_{SM}$

1.5. DESIGN EXAMPLE.

Table 1.1

The power circuit is designed to meet the following specification:

Output power	P_0=132W
Output voltage	V_0=160V
Output voltage ripple	<2%
Input voltage	V_{Seff}=110V, RMS
Input current ripple	≤5%
Switching frequency	f_{sw}=20kHz
Load resistance	R=212Ω
Input Inductance	$L=22.5mH$
Output Capacity	$C=940\mu F$

A. Design of L

The inductor current is controlled by two voltages; one is the rectified sinusoidal input voltage, which is applied to one side of the inductor, and the other one is the voltage across the switch, which varies between zero and v_0 due to switching and is applied to the other side of the inductor. The voltage that contributes to the ripple is the voltage across the switch. In other words, it can be said that the ripple current is produced by an equivalent wave of amplitude $V_0/2$ and frequency equal to the switching frequency. To consider the worst case for ripple, the duty cycle of the switch is taken to be 50% for this analysis. Based on the above assumptions, output voltage v_0, switching frequency f_{sw}, inductance value L, and *RMS* value of the fundamental component of current ripple at 50% duty cycle I_{1r} are related through the following:

$$\left(\frac{V_0}{2}\right)\left(\frac{4}{\pi\sqrt{2}}\right) = (2\pi f_{sw} L) I_{1r} \tag{1.12}$$

Note that $\left(\frac{V_0}{2}\right)\left(\frac{4}{\pi\sqrt{2}}\right)$ is the RMS value of the fundamental component of the switched voltage for a 50% duty cycle. In addition, the fundamental or switching frequency component of the current ripple represents more than 99% of the total RMS current generated by the square-wave voltage ripple.

The maximum permitted amount of ripple is 5%; therefore, $I_{1r}=0.05I_L$ (Where I_L is the RMS value of the100Hz component of the inductor current).Therefore.

$$L = \left(\frac{1}{\sqrt{2}\pi^2 0.05}\right)\left(\frac{V_0}{f_{sw} I_L}\right) = (1.437)\left(\frac{V_0}{f_{sw} I_L}\right) \tag{1.13}$$

With the values chosen before, L is found to be *6.59mH*.

From (1.13) it is very clear that to reduce L to the small values we must increase the switching frequency f_{sw}, the boost-type PFC converter tends to decrease the volumetric size and weight

B. Design of C

To find the value of C for a desired output voltage ripple, we note that the capacitor-resistor combination at the output of the converter acts as low-pass filter for the current through the boost diode. Considering, only its dc and fundamental components. Therefore

$$i_0(t) \cong k_0(1 - cos2\omega t) \tag{1.14}$$

By comparing (1.5) and (1.14) and with the ideal voltage loop (K_S=V_{SM}) k_0 is

$$K_0 = \frac{V_{SM}^2 I_{refDC}}{2K_s V_{0DC}} = \frac{V_{SM} I_{refDC}}{2V_{0DC}} \tag{1.15}$$

The gain of the filter for the dc component of the current i_0 is R and for the ac component is:

$$|G_{ac}| = \frac{R}{((2RC\omega)^2 + 1)^{1/2}} \tag{1.16}$$

Therefore

$$\tau_{ond} = 2\frac{|G_{ac}|}{G_{dc}} = \frac{2}{((2RC\omega)^2 + 1)^{1/2}} \tag{1.17}$$

Then

$$C = \frac{(4 - \tau_{ond}{}^2)^{1/2}}{2\tau_{ond} R\omega} \tag{1.18}$$

To get a ratio very less than *2%*, a capacitor with *C=940μF* would be adequate.

1.6. VOLTAGE-LOOP CONTROLLER.

The components of the *DC-DC* converter are being considered ideal. Under this assumption, the total instantaneous power will be independent from the instantaneous power of the converter. And assuming that $i_L \cong i_{ref}$

Where

$$P(1 - cos2\omega t) = v_0 i_D = v_0 \left(C \frac{dv_0}{dt} + \frac{v_0}{R} \right) \tag{1.19}$$

It is certain that the output voltage ripple at *100 Hz* is not interesting at all the calculation of the voltage controller whose bandwidth will be very weak (some hertz), to satisfy the constraint shape of the current i_L.

We can so, considering that the equation (1.19) established for the instantaneous power can be reduced to that of the average power. The essential difference will concern the disappearance of the ripple at*100 Hz* of this voltage, ripple due to the fluctuating power. The action of the controller will be to maintain the mean value of the output voltage and not the instantaneous value, (1.19) Becomes:

$$\frac{V_{SM} I_{refDC}}{2} \cong C \frac{dV_{0DC}^2}{dt} + \frac{V_{0DC}^2}{R} \tag{1.20}$$

The indication *DC* is used to remind that only the mean value of v_0 is expressed in this equation. As can be seen in (1.20), the regulation of V_{0DC} is made possible by action on the amplitude of I_{refM} fig.1.6. To calculate the controller parameters the above equation is nonlinear and is therefore linearized around the operating point defined by (V_{0DCC} and I_{refDCC})

The transfer function of the system $T_V(s)$ is obtained:

$$T_V(s) = \frac{\delta V_{0DC}}{\delta I_{refDC}} = \frac{V_{SM}}{4V_{0DCC}} \frac{R}{1 + RCs} \tag{1.21}$$

The voltage loop controller $C_V(s)$ is usually a first order lag given by the following parameters:

$$k_{PI} = \frac{RC}{T_{PI}}, T_{PI} = \frac{BRV_{SM}}{8\pi(f_{CV})V_{0DCC}} \tag{1.22}$$

Where

B: the attenuation of the measured output voltage,

f_{CV}: voltage closed loop crossover frequency.

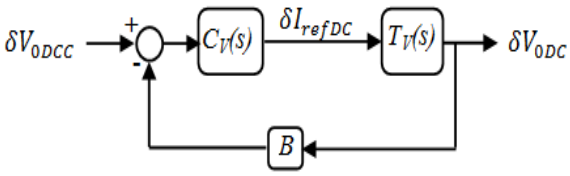

Fig.1.6 Voltage loop controller.

Pole and gain are chosen to obtain a sufficient phase margin gain *(≈45°)* and bandwidth in the *5* to *20 Hz* range. The bandwidth is intentionally kept very low since the compensator gain at *100 Hz* effectively determines the third harmonic to be expected in the input current. Since the outer loop has a finite dc gain, the voltage reference is pre-compensated to avoid a steady state voltage error at nominal operation.

1.7. CURRENT-LOOP CONTROLLER.

The boost PFCS of Fig.1.3 is nonreversible, so to avoid crossover distortion, it is essential that the phase difference between i_L and v_{in} is negligible. In cascade control structure, this requirement is satisfied if the current loop has excellent tracking. The full-wave rectified signal v_{in} has no significant harmonic content above 1 kHz. Therefore, adequate tracking should be possible with a current loop crossover frequency, f_{CI} *=5-10 kHz*. However, due to the nonlinear nature of (1.1), a linear controller cannot be used without i_L becoming distorted [10]. The distortion can be avoided if, in the closed loop, the state-space averaged input current dynamics are linear in the large. This can be achieved through the use of suitable nonlinear controller designed using formal feedback linearization methods [11]. In this case, the correct controller form for feedback linearization can be found by inspection:

Assuming that the output voltage is constant V_0, then equation (1.1) becomes

$$1 - d = \frac{1}{V_0}\left[\frac{2}{\pi}V_{SM} - C_I(s)\left(i_{ref} - i_L\right)\right] \tag{1.23}$$

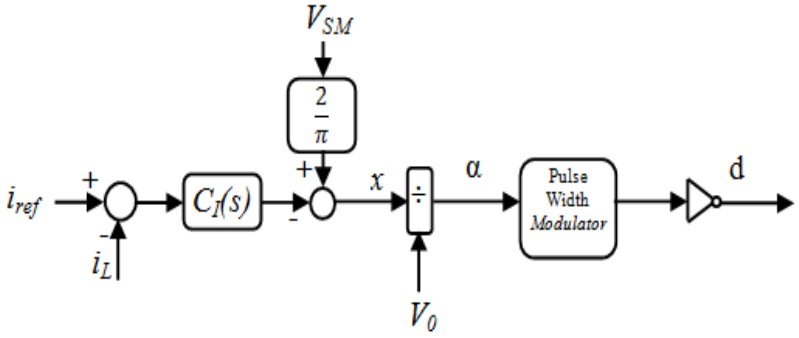

Fig.1.7. Current loop controller.

A block diagram of the controller is depicted in Fig 1.7. The state-space averaged open loop transfer function of the current loop is $C_I(s)T_I(s)$, Where the plant transfer function $T_I(s)$ is defined by.

$$T_I(s) = \frac{1}{sL} \tag{1.24}$$

The compensator $C_I(s)$ is designed to obtain an acceptable phase margin and a bandwidth of the order of *10* KHz

1.8. SIMULATION RESULTS.

A comprehensive simulation and real-time experimental study were performed to capture the performance of the proposed PI_PI control for single-phase power factor correction. First, the steady-state performance is evaluated in terms of output voltage regulation, THD, and power factor. Next, the transient performance is evaluated for output voltage response on application of load step changes that are expected in practical applications of this circuit.

1) steady-state *performance:* Fig.1.8 illustrates the simulated waveforms, dc-bus voltage, the line voltage, the line current and his associated spectrum (appropriately scaled for

easy viewing) in the steady-state with a unity power factor, for the PI_PI control at nominal load and nominal line voltage—these waveforms have been appropriately shifted in time to be visible. From this figure, it can be seen that the results obtained with the proposed PI_PI control are much better than the adoption of IEC 1000-3-2 [4] as the EN61000-3-2 norm in Europe and the formulation of the IEEE 519 [5] in the USA. Line current is very close to sine wave and in phase with the power source voltage—the THD is 2.97%. It is important to note that at nominal line and load condition, the PI_PI control has THD number below 3% even with the limited bandwidth that is allowed by the digital implementation. As far as steady-state error in the output voltage is concerned—the steady-state error is 1V.

2*) Transient* performance*:* As previously stated, step load changes are effected by connecting (or disconnecting) parallel load. The reference current amplitude is limited to *3.5A* in the control for the PI_PI control designs.

Fig.1.9 shows the transient response for the proposed PI_PI control for single-phase power factor correction for a load resistor step from *212*Ω to *312* Ω and from *312*Ω to *212* Ω. After a short transient, the dc-bus voltage is maintained close to its reference value with a good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 1.2.

The dynamic behavior of the proposed PI_PI under a step change of V^*_0 is presented in Fig.1.10. After a short transient, the dc-bus voltage is maintained close to its new reference with good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 1.3.

Fig. 1.11 shows the transient of the step change of v_s in the proposed PI_PI control by decreasing v_s from *150 V* to *140 V* and increasing them from *140 V* to *150 V*. After a short transient, the dc-bus voltage is maintained close to its new reference with good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 1.4.

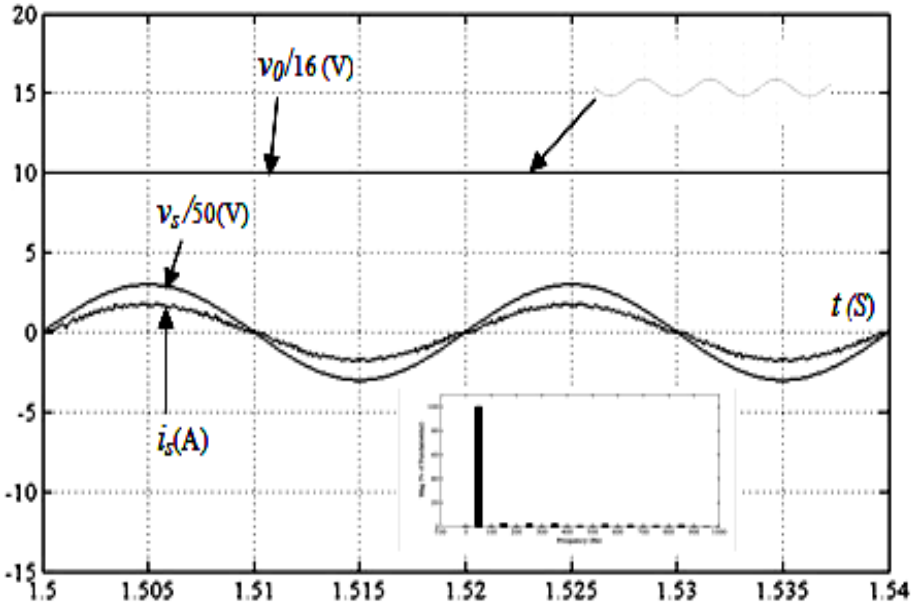

Fig.1.8 Simulated basic signal waveforms in steady state under UPF, $V^*_0=160$ V, $THD=2.97\%$.

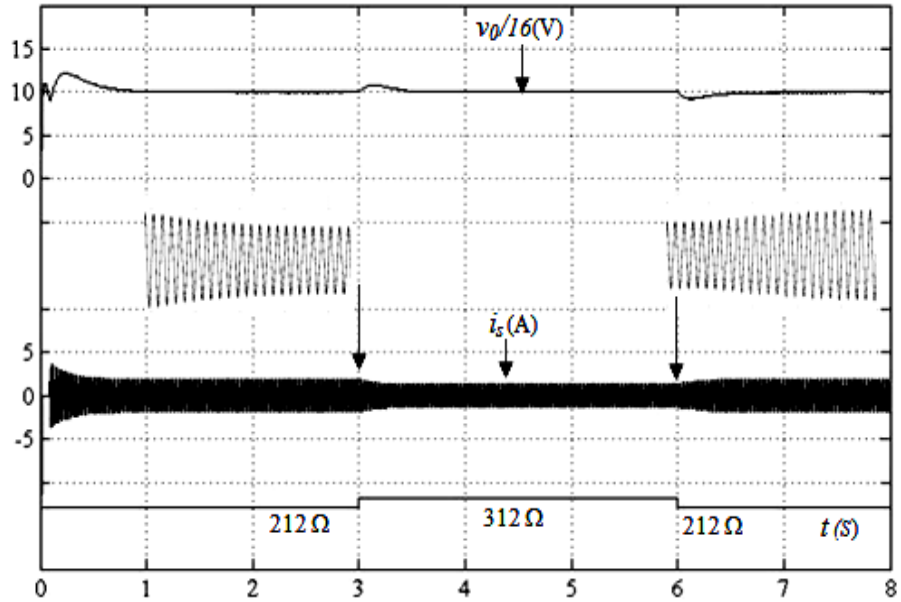

Fig. 1.9 Transient of the step change of the load Increasing from *212*Ω to *312*Ω and Decreasing from *312* Ω to *212*Ω.

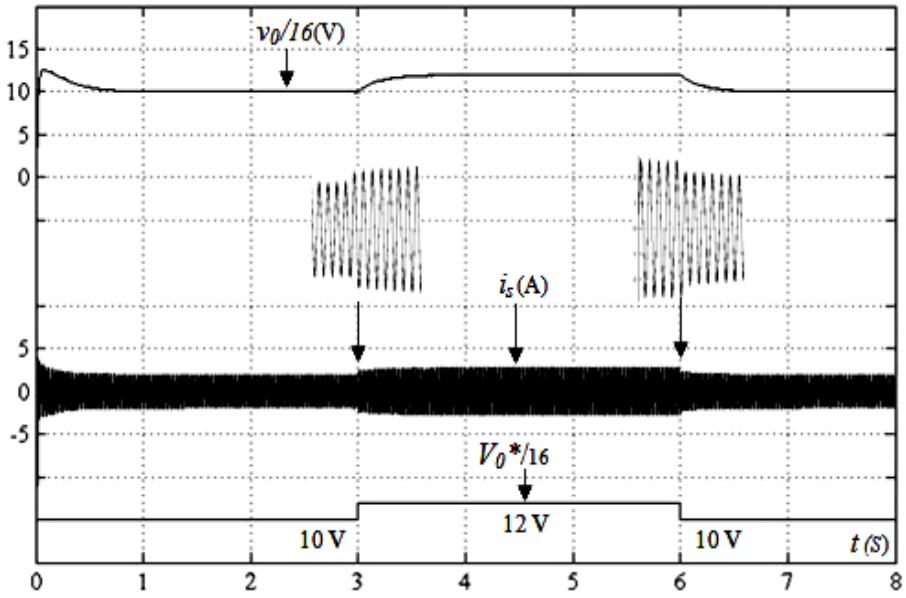

Fig. 1.10 Transient of the step change of V^*_0, Increasing from *160 V* to *192 V* and Decreasing from *192 V* to *160 V*.

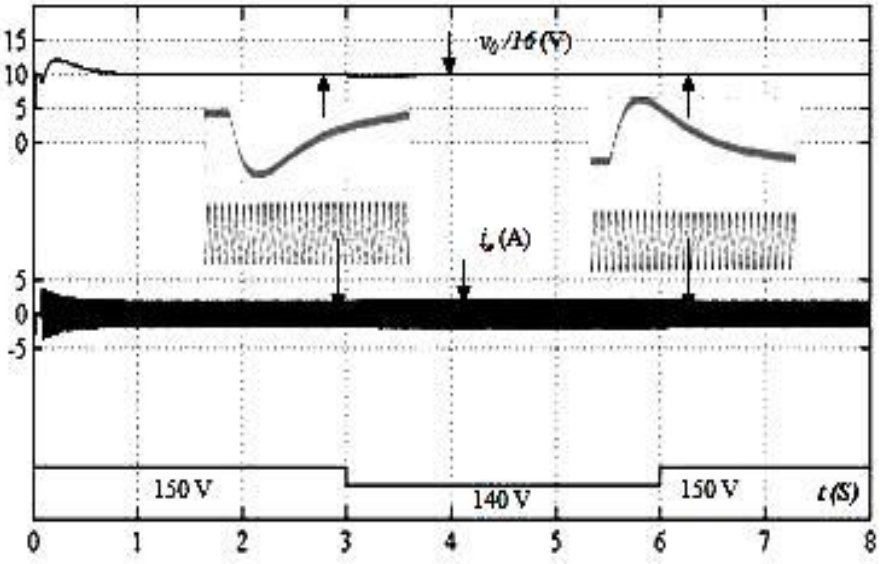

Fig. 1.11 Transient of the step change of v_s, decreasing from *150 V* to *140 V* and increasing from *140 V* to *150 V*.

Table1. 2

Transient values corresponding to Fig. 1.9.

Load	ΔV_0 *(V)*	Δt *(S)*	ΔI_{ref} *(A)*	Δt *(S)*
212Ω/312Ω	*12.8*	*0.7*	*0.52*	*0.5*
312Ω/212Ω	*12.8*	*0.7*	*0.52*	*0.5*

Table 1.3

Transient values corresponding to Fig.1. 10.

V^*_0	ΔV_0 *(V)*	Δt *(S)*	ΔI_{ref} *(A)*	Δt *(S)*
160V/192V	*32*	*0.8*	*0.7*	*1*
192V/160V	*32*	*0.8*	*0.7*	*1*

Table 1.4

Transient values corresponding to Fig.1. 11.

v_s	ΔV_s *(V)*	Δt *(S)*	ΔI_{ref} *(A)*	Δt *(S)*
150V/140V	*3.2*	*0.7*	*0.14*	*0.8*
140V/150V	*3.2*	*0.7*	*0.14*	*0.8*

1.9. CONCLUSION.

In this chapter, the simulation design constraints of power-factor-correction power supplies that use a cascading structure to achieve high power factor and fast regulation have been study. In addition, the small-signal model of the proposed converter was developed, from witch an optimal PI compensator is designed for the converter system with peak-current mode control. However, the input current harmonic content is very close to the limit. Simulations results have been shown that fast dynamic response; good output regulation, low harmonic distortion, and high power factor can be achieved with the proposed single-stage converter and control scheme.

REFERENCES.

[1] Yu Qin, Shanshan Du. "**Fuzzy logic and digital PI control of single phase power factor pre-regulator for an online UPS-a comparative study"** Industrial Technology, 1996. (ICIT apos; 96), Proceedings of The IEEE International Conference on Volume, Issue, 2-6 Dec 1996 pp. 103 – 107.

[2] Ahmed H. Mitwali, Steven B. Leeb, George C. Verghese and V. Joseph Thottuvelil. **"An Adaptive Digital Controller for a Unity Power Factor Converter,"** IEEE Transaction on Power Electronics, vol. 11, no. 2, pp. 374–382, March 1996.

[3] Simon Wall and Robin Jackson**. "Fast Controller Design for Single-Phase Power-Factor Correction Systems,"** IEEE Transaction on Industrial Electronics, vol. 44, no. 5, pp. 654–660, October 1997.

[4] Tsai-Fu Wu and Yu-Kai Chen. **"Analysis and Design of an Isolated Single-Stage Converter Achieving Power-Factor Correction and Fast Regulation,"** IEEE Transaction on Industrial Electronics, vol. 46, no. 4, pp. 759–767, August 1999.

[5] Jee-Woo Lim and Bong-Hwan Kwon. **"A Power-Factor Controller for Single Phase PWM Rectifier,"** IEEE Transaction on Industrial Electronics, vol. 46, no. 5, pp. 1035–1037, October 1999.

[6] Zaohong Yang and Paresh C. Sen. **"A Novel Technique to Achieve Unity Power Factor and Fact Transient Response In Ac-to-Dc Converters,"** IEEE Transaction on Power Electronics, vol. 16, no. 6, pp. 764–78, Novembre 2001.

[7] Fu M. Chen Q**. "Applied Power Electronics Conference and Exposition"**, 2001, APEC, 2001, Sixteenth Annual IEEEVolume 1, Issue, 2001 pp. 144 - 149 vol.1.

[8] Masashi Ochiai and Hirofumi Matsuo. **"An AC/DC Converter with High Power Factor**," IEEE Transaction on Industrial Electronics, vol. 50, no. 2, pp. 356–361, April 2003.

[9] Diego G. Lamar, Arturo Fernandez, Manuel Arias. "**A Unity Power Factor Correction Preregulator With Fast Dynamic Response Based on a Low-Cost Microcontroller"** IEEE Transaction on Power Electronics, vol. 23, no. 2, pp. 635–641, March 2008.

[10] Martin K. H. Cheung, Martin H. L. Chow, Chi K. Tse. **"Practical Design And Evaluation of A 1 KW PFC Power Supply Based en Reduced Redundant Power Processing Principle**," IEEE Transaction on Industrial Electronics, vol. 55, no. 2, pp. 665–673, February 2008.

[11] Vishnu Murahari Rao, Amit Kumar Jain, Kishore K. Reddy and Aman Behal. **"Experimental Comparison of Digital Implementation of Single-Phase PFC Controllers**," IEEE Transaction on Industrial Electronics, vol. 55, no. 1, pp. 67–78, January 2008.

[12] John Chi Wo Lam and Praveen K Jain. **"A Modified Valley Fill Electronic Ballast Having a Current Source Resonant Inverter With Improved Line- Current Total Harmonic Distortion (THD), High Power Factor, and Low Lamp Crest Factor**," IEEE Transaction on Industrial Electronics, vol. 55, no. 3, pp. 1147–1159, March 2008.

CHAPTER 2

PI-HYSTERESIS CONTROL FOR ACTIVE

POWER FACTOR CORRECTION

Abstract—*this Chapter presents a modeling approach to obtain a small-signal model and the simulation of a PI controller in the loop voltage and two controllers in the loop current based first on a standard fixed and sinusoidal band hysteresis control, followed by a variable band hysteresis control for a single-phase power factor corrector (PFC). All these controllers have been verified via simulation in Simulink using a continuous time plant model and a discrete time controller. All these controllers are compared for steady-state performance and transient response. It is shown that the PI controller gives a better steady-state performance under large load disturbance and plant uncertainties, whereas the variable band hysteresis control in the loop current gives a low THD of the input current compared to a standard classical fixed and sinusoidal band hysteresis control.*

2.1. INTRODUCTION.

Single-phase power factor correction (PFC) circuits provide rectification of the line voltage to a regulated dc voltage while shaping the input current to be a sinusoid and in phase with the line voltage [1]. Often, the PFC acts as a preregulator to a dc–dc converter that may be used to provide additional regulation and ohmic isolation [2], [3]. Due to adoption of IEC 1000-3-2 [4] as the EN61000-3-2 norm in Europe and the formulation of the IEEE 519 [5] in the USA, these circuits are increasingly being used in the front-end of electronic equipment. Among the several possible topologies [2], the boost PFC shown in Fig. 2.1 is most commonly used. The control objectives are to track the inductor current to a rectified Sinusoid (so that the line current is sinusoidal and in phase with the line voltage) and to regulate the average output voltage to a desired magnitude and to has a fast response to the load variation [6], [7].

Commonly, a linear controller (PI-PI controller) is designed utilizing a small-signal model that is obtained by linearization about an operating point [6] in both, outer loop for output dc voltage regulation (loop voltage) and inner loop so that the line current is sinusoidal and in phase with the line voltage (loop current). The system provides acceptable performance. In [9], a PI control scheme is presented that includes a 100 Hz notch filter in the voltage control loop. The notch filter reduces the amount of second harmonic that is reaching the multiplier. Thus, the voltage loop bandwidth can be increased, which leads to a faster transient response, without the penalty of increased third harmonic in line current in steady state. The improvement in the transient response of the loop voltage controller degrades the quality of the input current (High THD). On the other hand, PI controller design in loop current requires an accurate mathematical model of the plant and it failed to perform satisfactorily under parameter

variation, nonlinearity (two multiplications), load disturbance, etc [10]. Hysteresis current controller (bang-bang hysteresis (BBH) technique) has an advantage in coping with the time varying nonlinearity of switches in PFC pre-regulator, and it does not require an accurate mathematical model of the PFC pre-regulator when the controller is being designed [11]. Also this technique has an advantage of yielding instantaneous current control [12], which results in very fast response and increased 'boost' switch reliability. However, it has a serious disadvantage in that the switching frequency of the boost switch f_{sw} is not constant and varies in a wide range during each half cycle of the ac input voltage[13], [14]. The switching frequency is also sensitive to circuit component values, design parameters and difficult for EMI filter design. The novel feature of the proposed method resides in the fact that unity power factor and nearly sinusoidal inputs current are obtained at constant switching frequencies [15] [16]. Moreover, the method exhibits instantaneous current control, which results in very fast response and increased switch reliability.

This chapter presents a systematic design, and simulation comparison: 1) of a PI controller with a 100 Hz notch filter for a voltage loop of a regulated dc voltage, 2) standard hysteresis controller and redesign of the standard hysteresis controller with some modifications for improved performance for a current loop. All these controllers are verified by detailed MATLAB/Simulink based simulations through the use of a continuous time plant model and a discrete time controller. These controllers are compared for steady-state performance and transient response over the entire range of input and load conditions for which the system is designed. The chapter is organized as follows. In Section 2.1, we describe the system dynamics and lay down the control objectives. Sections 2.2 and 2.3 present the design and analysis for the outer and inner controllers. Section 2.4 and 2.5 presents the details of the simulations and results. Section 2.6 concludes with discussions of the results.

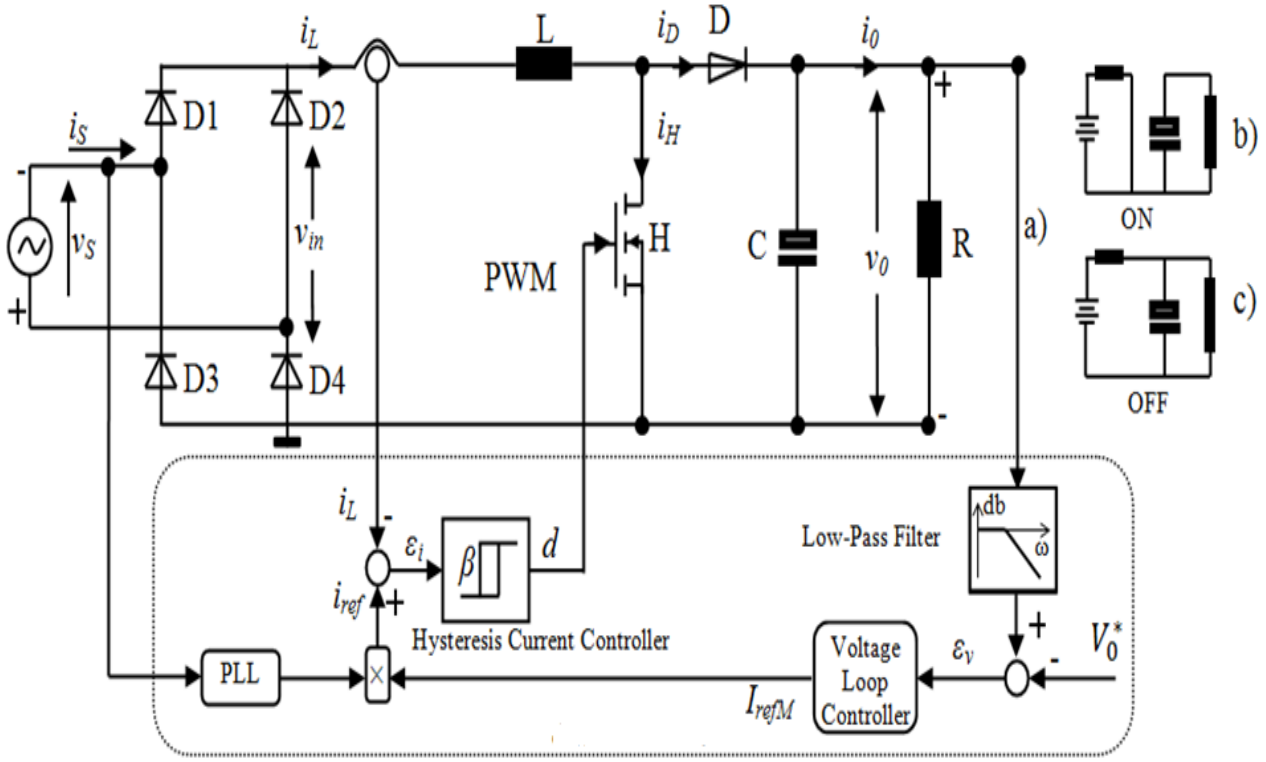

Fig.2.1. PFC preregulator.

2.2. VOLTAGE-LOOP CONTROLLER.

As shown in Fig.2.2, the dc-bus voltage v_0 is sensed and compared with a reference value V_0^*. The obtained error is used as input for the PI controller, the output of the controller I_{refM} multiplied by $sin\omega t$ obtained from PLL stage with sensing of the input voltage is the instantaneous reference current command i_{ref}.

The system in Fig. 1.1 is modeled as a first order system:

$$\frac{v_0}{I_{refM}} = \frac{V_{SM}}{4V_0^*}\frac{R}{1+\frac{RC}{2}p} = \frac{k_s}{1+\tau_s p} \tag{2.1}$$

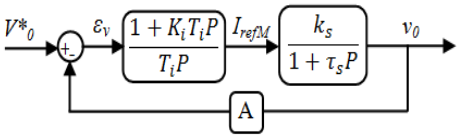

Fig.2.2 PI controller structure using for hysteresis.

The transfer function of the PI controller is: $\frac{1+K_i T_i P}{T_i P}$

The PI parameters are chosen as: $K_i = \frac{RC}{2T_i}, T_i = \frac{ARV_{SM}}{8\pi f_{CV} V_0^*}$

Where

f_{CV}: voltage closed loop crossover frequency.

With f_{CV}*=10Hz*, then K_i*=2.0160* and T_i*=0.0494*.

Then the closed loop transfer function with the design example given in table 2.1 is:

$$\frac{v_0}{V_0^*} == \frac{k_F}{1+\tau_F p} = \frac{16}{1+0,0159p} \tag{2.2}$$

The power circuit is designed to meet the following specification:

Table 2.1

Design specification and circuit parameters.

Switching frequency	f_{sw}*=20kHz*
Output power	P_0*=121W*
AC amplitude of supply voltage	V_{SM}*=150V*
DC output voltage	V_0*=160V*
Input current ripple	*≤2.5%*
Output voltage ripple	*≤2%*
Load resistance	*R=212*Ω
Input Inductance	*L=22.5mH*
Output Capacity	*C=940μF*

Fig.2.3 show the Bode plot of the voltage controlled system.

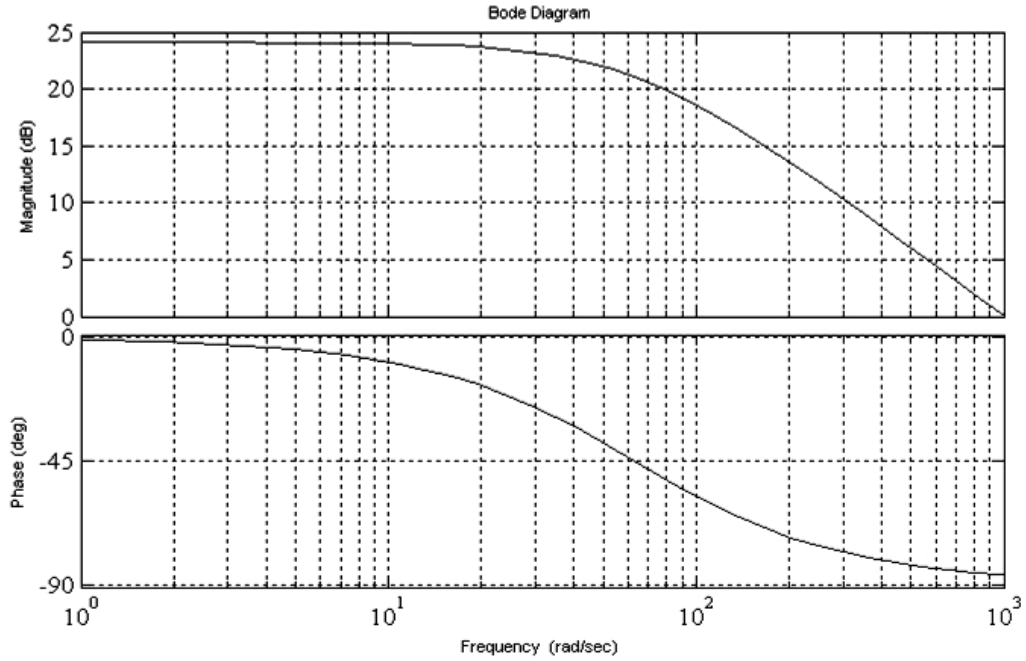

Fig.2.3 Bode plot of the voltage controlled system

Pole and gain are chosen to obtain a sufficient phase margin gain *(≈45°*) and bandwidth in the *5* to *20 Hz* range. The bandwidth is intentionally kept very low since the compensator gain at *100 Hz* effectively determines the third harmonic to be expected in the input current. Since the outer loop has a finite dc gain, the voltage reference is pre-compensated to avoid a steady state voltage error at nominal operation.

2.3. CURRENT-LOOP CONTROLLER.

The Single-phase power factor correction (PFC) circuit analyzed here has a feedback loop such that the switching mode is determined by comparison of the actual current and sinusoidal reference current supplied form voltage loop controller in both ways the actual current in the first oscillates in fixed band hysteresis (FBH), in the second way oscillates in sinusoidal band hysteresis (SBH) as shown in Fig.2.4. And in the third way the actual current oscillates in variable band hysteresis (VBH).

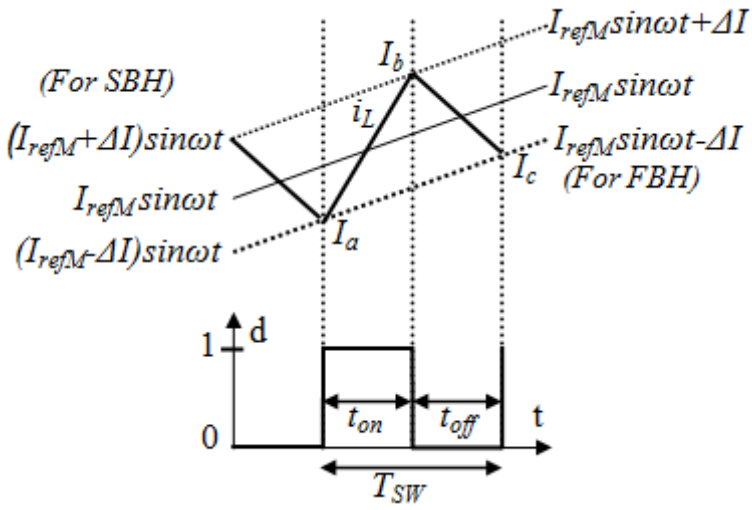

Fig.2.4 Switching frequency.

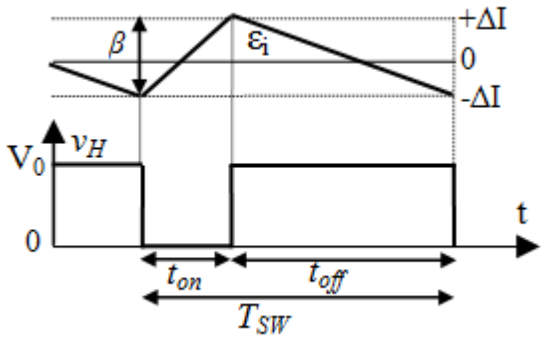

Fig.2.5 Current error and the switch H voltage.

A. CONVENTIONAL HYSTERESIS CURRENT CONTROL.

1. Fixed Band Control.

In this scheme, the hysteresis bands are fixed throughout the fundamental period. The algorithm for this scheme is given as:

Upper band $(i_{upper}) = I_{refM}\sin\omega t+\Delta I = I_{refM}\sin\omega t+\beta/2$

Lower band $(i_{lower}) = I_{refM}\sin\omega t-\Delta I = I_{refM}\sin\omega t-\beta/2$

Where $\beta=2\Delta I$ is band hysteresis.

If $i_L > i_{upper}$, d=0 then, $v_H=V_0$

If $i_L < i_{lower}$, d=1 then, $v_H=0$

2. Sinusoidal Band Control.

In this scheme, the hysteresis bands are sinusoidal throughout the fundamental period. The algorithm for this scheme is given as:

Upper band $(i_{upper}) = (I_{refM} + \Delta I)\ sin\omega t = (I_{refM} + \beta/2) sin\omega t$

Lower band $(i_{lower}) = (I_{refM} - \Delta I)\ sin\omega t = (I_{refM} - \beta/2)\ sin\omega t$

Where $\beta = 2\Delta I$ is band hysteresis.

If $i_L > i_{upper}$, d=0 then, $v_H = V_0$

If $i_L < i_{lower}$, d=1 then, $v_H = 0$

3. Control characteristics.

To investigate the control characteristics of a single-phase power factor corrector (PFC), the variation of maximal switching frequency with the inductance L of ΔI parameter for both techniques FBH and SBH is evaluated as seen in Fig.2.6. From Fig.2.4 and (2.5), by considering the output voltage V_0 constant over a switching period we can write:

$$t_{on} = \frac{L}{v_{in}}(I_b - I_a), t_{off} = \frac{L}{v_{in} - V_0}(I_c - I_b) \tag{2.3}$$

Then the switching frequency is:

$$f_{sw} = \frac{1}{T_{SW}} = \frac{1}{t_{on} + t_{off}} \tag{2.4}$$

From Fig.2.1, the v_H voltage is given by the following equation:

$$v_{in} - L\frac{di_L}{dt} = v_H \tag{2.5}$$

For the ideal PFC operation, we can assume the current i_L to the reference rectifier sinusoidal shape i_{ref}, and then equation (2.5) becomes:

$$v_{in} - L\frac{di_{ref}}{dt} = v_H^* \tag{2.6}$$

From (2.5) and (2.6), we obtained

$$L\frac{d\varepsilon_i}{dt} = v_H - v_H^* \tag{2.7}$$

Where:

$\varepsilon_i = i_{ref} - i_L$: is the error current in the band of the hysteresis,

v_H^* : is the interrupter reference voltage corresponding to the ideal PFC operation.

From (2.7), if we assume the quantity $v_H - v_H^*$ constant during the switching period, then the error current $\varepsilon_i(t)$ varied as triangular form as shown in Fig.2.5

t_{on} and t_{off} obtained above in (3), can be find with another form using Fig.2.4 and equation (2.7):

$$t_{on} = \frac{L\beta}{v_H^*}, t_{off} = \frac{L\beta}{V_0 - v_H^*} \tag{2.8}$$

$$f_{sw} = \frac{v_H^*(V_0 - v_H^*)}{L\beta V_0} \tag{2.9}$$

From (2.6) and (2.8), the switching frequency can be obtained by the following equation:

$$f_{sw} = \frac{\left(V_{SM}|\sin(\omega t)| - L\omega I_{refM}|\cos(\omega t)|\right)\left(V_0 - V_{SM}|\sin(\omega t)| + L\omega I_{refM}|\cos(\omega t)|\right)}{LV_0\beta} \tag{2.10}$$

Where:

$v_{in} = V_{SM}|\sin(\omega t)|$

$i_{ref} = I_{refM}|\sin(\omega t)|$

From the equality $\frac{df_{SW}}{d\omega t} = 0$, we find the maximal switching frequency with the inductance L of ΔI parameter shown in Fig.2.6.

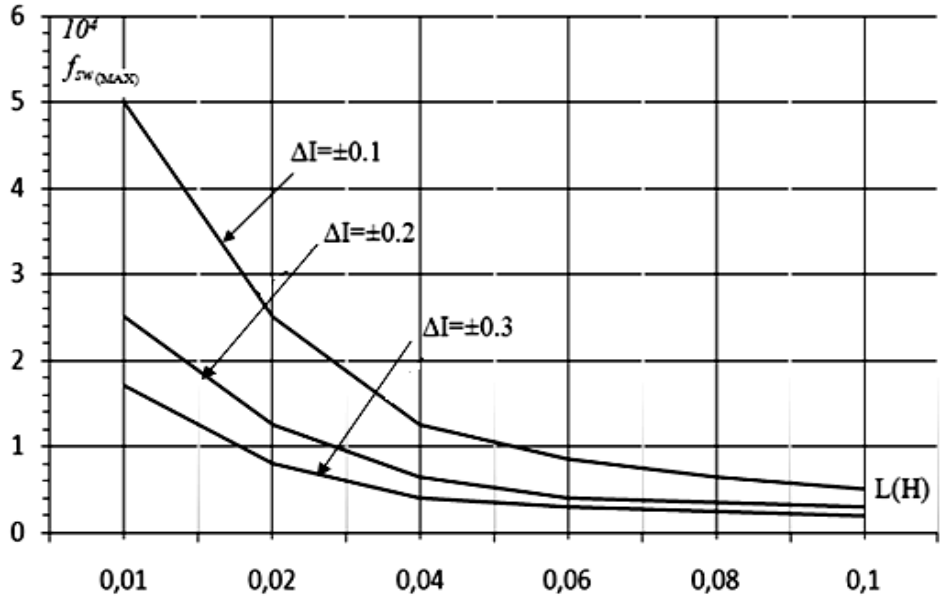

Fig 2.6 Variation of maximal switching frequency with L.

Fig.2.6 shows the variation of switching frequency (MSF) with inductance L for Δi parameter for the both techniques FBH and SBH. The network of curves $(f_{SW})_{MAX}=f(L)$ of parameter Δi for FBH, informs us about the value of L to choose to limit the excursion in frequency to a compatible value. With *0.1H* the maximal switching frequency is *5 kHz*. This relatively low frequency shows well the control by hysteresis. A more realistic simulation with *L=0.0225H* and thus a maximal switching frequency of *20 kHz* would allow faster variations of current i_L around his reference current i_{ref}. In addition, we note that the MSF with the sinusoidal bands controller is higher than the corresponding fixed bands controller over a full range of inductance *L*. For the same value of *L=0.0225H* the MSF is *25 kHz.*

B. HYSTERESIS CURRENT CONTROL WITH CONSTANT SWITCHING FREQUENCY.

From equation (2.10), if β is constant and the time t varies, then the switching frequency f_{SW} also varies. To get a constant switching frequency f_{SW}, the hysteresis bands have to be dynamically changes, according to this equation:

$$\beta = \frac{\left(V_{SM}|\sin(\omega t)| - L\omega I_{refM}|\cos(\omega t)|\right)\left(V_0 - V_{SM}|\sin(\omega t)| + L\omega I_{refM}|\cos(\omega t)|\right)}{LV_0 f_{swd}} \quad (2.11)$$

Where, f_{swd} is the desired switching frequency.

Equation (2.11) gives a very simple control law with constant switching frequency allowing the improvement of characteristics of hysteresis current controller in terms of switching loss, audible noise and EME related problems.

2.4. SIMULATION RESULTS.

Comprehensive simulations studies were performed to capture the performance of the proposed PI_Hysteresis control for single-phase power factor correction. First, the steady-state performance is evaluated in terms of output voltage regulation, THD, and power factor. Next, the transient performance is evaluated for output voltage response on application of load step changes and reference voltage step that are expected in practical applications of this circuit.

1) steady-state performance: Figs.2.7, 2.8 and 2.9 illustrate the simulated waveforms, dc-bus voltage, the line voltage, the line current and his associated spectrum (appropriately scaled for easy viewing) in the steady-state with a unity power factor, for the PI_Hysteresis control, FBH, SBH and VBH, respectively at nominal load and nominal line voltage—these waveforms have been appropriately shifted in time to be visible. From these figures, it can be seen that the results obtained with the proposed PI_Hsteresis control are much better than the adoption of IEC 1000-3-2 [4] as the EN61000-3-2 norm in Europe and the formulation of the IEEE 519 [5] in the USA. Line current is very close to sine wave and in phase with the power source voltage—the THD in the three hysteresis techniques control is less than 4%. It is important to note that at nominal line and load condition, the PI_Hysteresis control with variable band hysteresis has THD number about 2,01% even with the limited bandwidth that is allowed by the digital simulation. With the variable band hysteresis control the THD of the input current is much better then with the fixed band hysteresis control. As far as steady-state error in the output voltage is concerned—the steady-state error is 2V.

2*) Transient performance:* As previously stated, step load changes are effected by connecting (or disconnecting) parallel load. The reference current amplitude is limited to *3.5A* in the control for the PI_Hystersis control designs.

Fig.2.10 shows simulations results of the transient response for the proposed PI_Hysteresis control for single-phase power factor correction for a load resistor step from *212*Ω to *312* Ω and from *312*Ω to *212* Ω. After a short transient, the dc-bus voltage is maintained close to its reference value with a good approximation and stability. The line currents have nearly sinusoidal waveforms and in phase with the input voltage. The corresponding transient values are shown in table 2.2.

The dynamic behavior of the proposed PI_Hysteresis under a step change of V^*_0 is presented in Fig.2.11. After a short transient, the dc-bus voltage is maintained close to its new reference with good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 2.3.

In the Fig. 1.12 the transient of the step change of v_s, by decreasing from 150 V to 140 V and increasing from 140 V to 150 V of the dynamic behavior of the proposed PI_Hysteresis. After a short transient, the dc-bus voltage is maintained close to its new reference with good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 2.4.

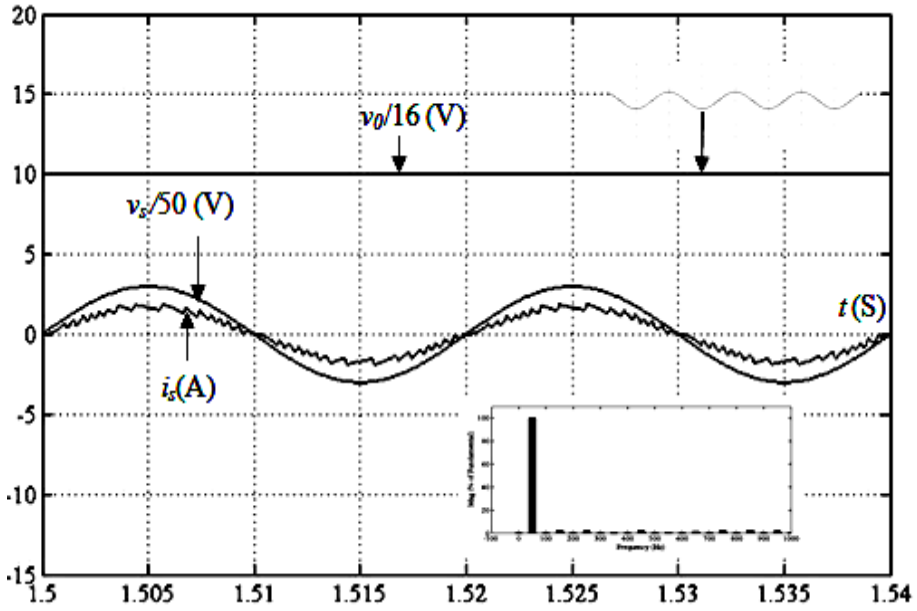

Fig.2.7 Simulated basic signal waveforms in steady state
under UPF, with FBH, *V*0=160 V, THD=3.98%*

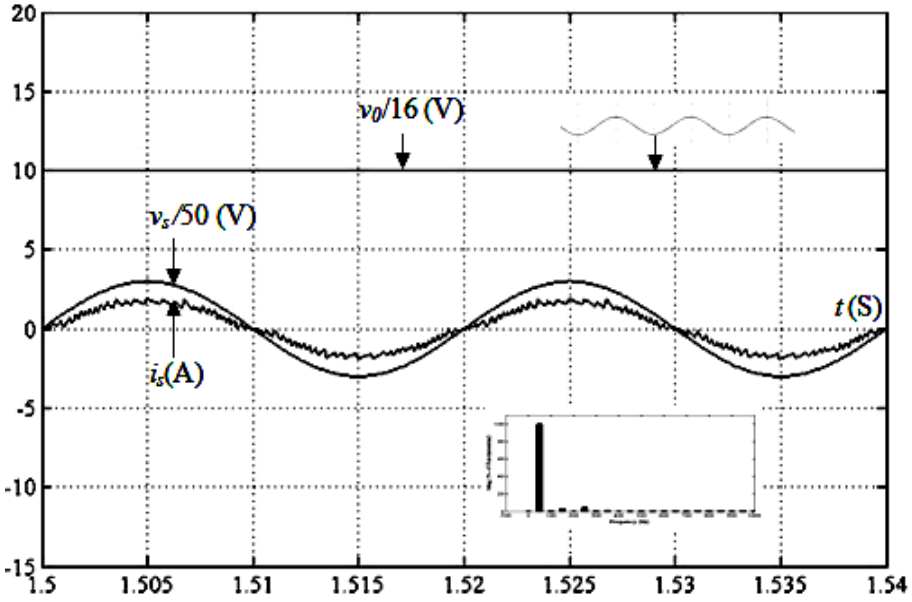

Fig.2.8 Simulated basic signal waveforms in steady state

. under UPF, with SBH, V^*_0=160 V, THD=3.17%.

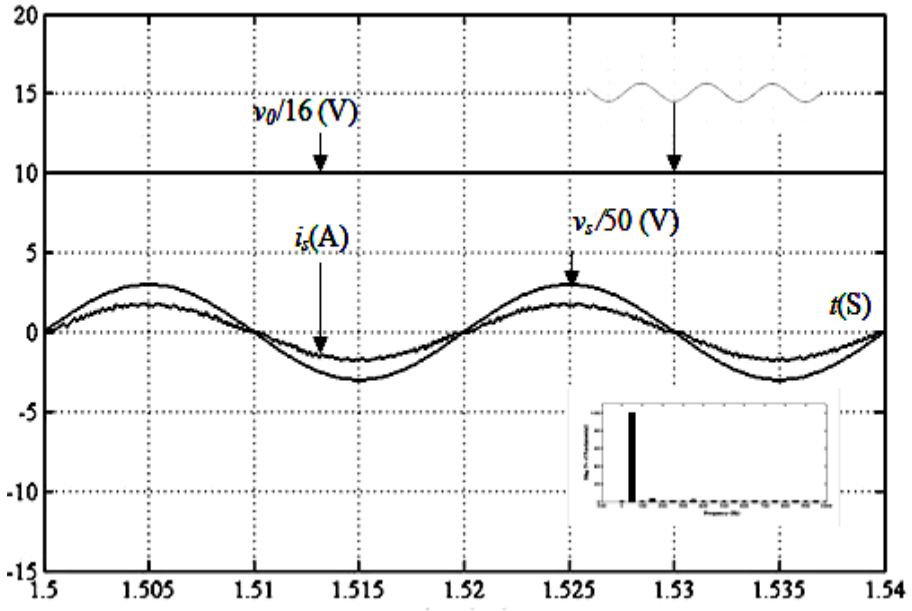

Fig.2.9 Simulated basic signal waveforms in steady state under UPF, with variable Band, V^*_0=160 V, THD=2.01%.

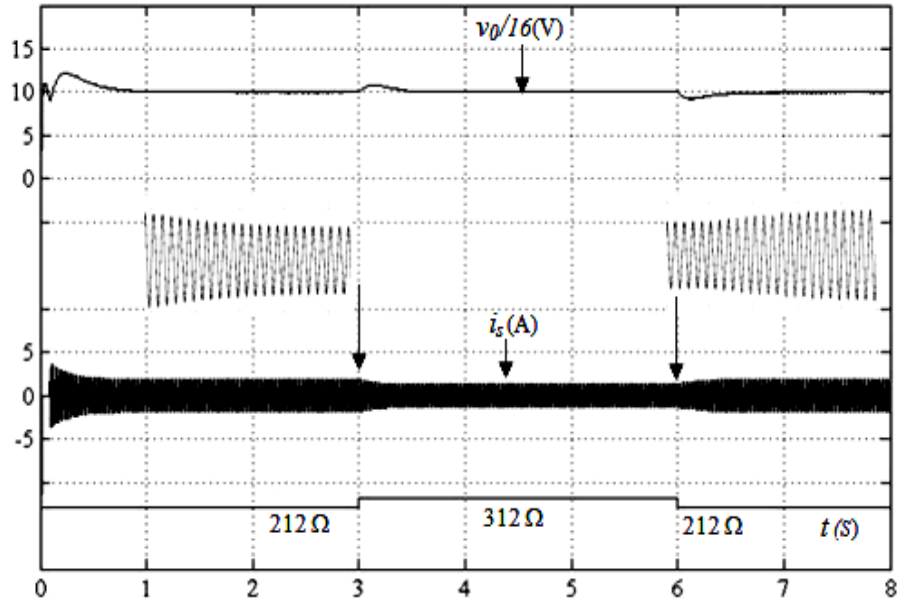

Fig.2.10 Transient of the step change of the load Increasing from 212Ω to 312Ω and Decreasing from 312 Ω to 212Ω.

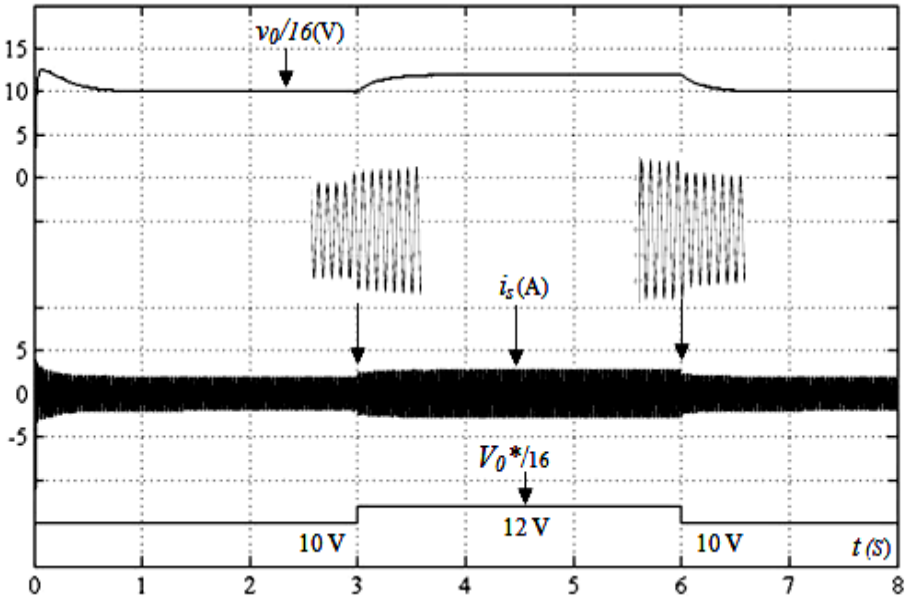

Fig. 2.11 Transient of the step change of V^*_0, Increasing from *160 V* to *192 V* and Decreasing from *192 V* to *160 V*.

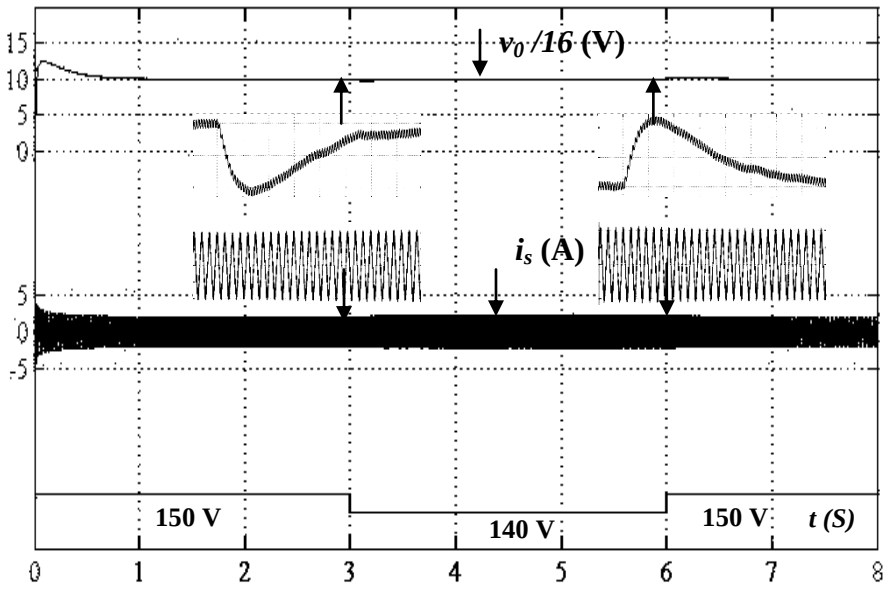

Fig. 2.12 Transient of the step change of v_s, decreasing from *150 V* to *140 V* and increasing from *140 V* to *150 V*.

Table 2.2

Transient values corresponding to Fig 2.10.

Load	*ΔV_0 (V)*	*Δt (S)*	*ΔI_{ref} (A)*	*Δt (S)*
212Ω/312Ω	*12.8*	*0.7*	*0.52*	*0.5*
312Ω/212Ω	*12.8*	*0.7*	*0.52*	*0.5*

Table 2.3

Transient values corresponding to Fig 2.11.

V^*_0	*ΔV_0 (V)*	*Δt (S)*	*ΔIref (A)*	*Δt (S)*
160V/192V	*32*	*0.8*	*0.7*	*0.8*
192V/160V	*32*	*0.8*	*0.7*	*0.8*

Table 2.4

Transient values corresponding to Fig 2.12.

v_s	*ΔV_0 (V)*	*Δt (S)*	*ΔIref (A)*	*Δt (S)*
150V/140V	*3.2*	*0.8*	*0.18*	*0.7*
140V/150V	*3.2*	*0.6*	*0.18*	*0.71*

2.5. CONCLUSION.

In this chapter, the design constraints of power-factor-correction power supplies that use a PI-Hysteresis control to achieve high power factor and fast regulation have been study. In addition, the small-signal model of the proposed converter was developed, from witch an optimal PI compensator is designed for the converter system with peak-current mode control. However, the input current harmonic content is very close to the limit specified in IEEE6519 Standard. The static performances of the variable band hysteresis controller are compared to those of the Fixed band hysteresis controller. The results show that the VBH control has THD of the input current much better then with the fixed band hysteresis control.

REFERENCES.

[1]. Yu Qin, Shanshan Du. "**Fuzzy logic and digital PI control of single phase power factor pre-regulator for an online UPS-a comparative study"** Industrial Technology, 1996. (ICIT apos; 96), Proceedings of The IEEE International Conference on Volume, Issue, 2-6 Dec 1996 pp. 103 – 107.

[2]. Ahmed H. Mitwali, Steven B. Leeb, George C. Verghese and V. Joseph Thottuvelil. **"An Adaptive Digital Controller for a Unity Power Factor Converter,"** IEEE Transaction on Power Electronics, vol. 11, no. 2, pp. 374–382, March 1996.

[3]. Simon Wall and Robin Jackson. **"Fast Controller Design for Single-Phase Power-Factor Correction Systems**," IEEE Transaction on Industrial Electronics, vol. 44, no. 5, pp. 654–660, October 1997.

[4]. Tsai-Fu Wu and Yu-Kai Chen**. "Analysis and Design of an Isolated Single-Stage Converter Achieving Power-Factor Correction and Fast Regulation**," IEEE Transaction on Industrial Electronics, vol. 46, no. 4, pp. 759–767, August 1999.

[5]. Jee-Woo Lim and Bong-Hwan Kwon. **"A Power-Factor Controller for Single Phase PWM Rectifier**," IEEE Transaction on Industrial Electronics, vol. 46, no. 5, pp. 1035–1037, October 1999.

[6]. Zaohong Yang and Paresh C. Sen. **"A Novel Technique to Achieve Unity Power Factor and Fact Transient Response In Ac-to-Dc Converters**," IEEE Transaction on Power Electronics, vol. 16, no. 6, pp. 764–78, Novembre 2001.

[7]. Fu M. Chen Q. **"Applied Power Electronics Conference and Exposition**"**,** 2001, APEC, 2001, Sixteenth Annual IEEE Volume 1, Issue, 2001 pp. 144 - 149 vol.1.

[8]. [8] Masashi Ochiai and Hirofumi Matsuo. **"An AC/DC Converter with High Power Factor**," IEEE Transaction on Industrial Electronics, vol. 50, no. 2, pp. 356–361, April 2003.

[9]. [9] L.Rahmani, F.Krim, A.Bouafia. **"Deadbeat Control for PWM AC Chopper,**" Taylor & Francis, Electric Power Components and systems, 32:453-466, 2004.

[10]. [10] L.Rahmani, F.Krim, M.S.Khanniche, A.Bouafia**. "Control for PWM AC Chopper feeding nonlinear loads,**" Taylor & Francis, INT. J. ELECTRONICS, Vol 91, No 3, March 2004, 149-163.

[11]. Diego G. Lamar, Arturo Fernandez, Manuel Arias. "**A Unity Power Factor Correction Preregulator With Fast Dynamic Response Based on a Low-Cost Microcontroller,"** IEEE Transaction on Power Electronics, vol. 23, no. 2, pp. 635–641, March 2008.

[12]. Martin K. H. Cheung, Martin H. L. Chow, Chi K. Tse. **"Practical Design And Evaluation of A 1 KW PFC Power Supply Based en Reduced Redundant Power Processing Principle**," IEEE Transaction on Industrial Electronics, vol. 55, no. 2, pp. 665–673, February 2008.

[13]. Vishnu Murahari Rao, Amit Kumar Jain, Kishore K. Reddy and Aman Behal. **"Experimental Comparison of Digital Implementation of Single-Phase PFC Controllers**," IEEE Transaction on Industrial Electronics, vol. 55, no. 1, pp. 67–78, January 2008.

[14]. John Chi Wo Lam and Praveen K Jain. **"A Modified Valley Fill Electronic Ballast Having a Current Source Resonant Inverter With Improved Line- Current Total Harmonic Distortion (THD), High Power Factor, and Low Lamp Crest Factor**," IEEE Transaction on Industrial Electronics, vol. 55, no. 3, pp. 1147–1159, March 2008.

[15]. N. Belhouchet and L.Rahmani. **"Development of Adaptative Hysteresis-band Current Control of PWM Three-Phase AC Chopper with Constant Switching Frequency,**" Taylor & Francis, Electric Power Components and systems, 37:583-598, 2009.

[16]. N. Belhouchet, L.Rahmani and S. Begag. "**A novel adaptative HBCC technique for three-phase shunt APF,**" Elsevier, Electric Power Systems Research, 79, 2009, 1097-1104.

CHAPTER 3

FUZZY LOGIC CONTROL FOR ACTIVE

POWER FACTOR CORRECTION

Abstract—*this Chapter presents a modeling approach to obtain a small-signal model and the simulation of a fuzzy logic controller in the loop voltage and hysteresis controller in the loop current for a single-phase power factor corrector (PFC). These controllers have been verified using simulation in Simulink using a continuous time plant model and a discrete time controller. These controllers are compared for steady-state performance and transient response. The proposed approach avoids complexities associated with non-linear mathematical modeling of switching converters. The control action is primarily derived from a set of linguistic rule written in accordance to experience and intuitive reasoning.*

3.1. INTRODUCTION.

During the twenties Jan Lukasiewicz proposed a trivalent logic (0, 0.5, 1), unlike traditional bivalent logic (0, 1). Then in the sixties Lotfi A. Zadeh expanded the theory and introduced the term "fuzzy". The most important features fuzzy logic is the use of natural language terms (such as high and low) instead of numerical values. These terms can be represented by fuzzy sets, which allow an element, differently in respect to traditional logic, to partially belong to more than one set [1]-[2].

This fuzzy approach offers the possibility to model a non–linear system on the basis of the knowledge of many non-well defined relations among the variables of the system, and to design a controller that adapts itself to several working conditions.

Power electronic systems are non-linear and time varying plants from a control system point of view:

1. Non-linear because the switch condition (that is the input of the controlled system) and the state of the system are multiplied between them. Moreover, when some devices are connected to the power electronic equipment (such as non-linear loads) there could be several non-linear relations between the system variables.

2. Time variant because the parameters of the system change with the temperature and the magnetic saturation.

Additionally there are dead-time effects, switch voltage drops and other unmodelled non-linearities. In addition, also considerable measurement noise should be included, finally, to increase the reliability and lower the cost of the system; there is a need to cut some

measurements and their associated cost: this has led to the development of so-called sensorless control schemes.

Thus, fuzzy logic seems a suitable solution both to model and to control power electronic systems [3].

3.2. FUZZY LOGIC BASED CONTROL.

A fuzzy logic controller (FLC) is based on a collection of control rules governed by the compositional rule of inference (Fig 3.1). A fuzzy system realizes a not linear correspondence between a vectorial and a scalar output [4]-[5], through the following steps:

1. Fuzzyfication
2. Inference
3. Knowledge basis
4. Defuzzyfication

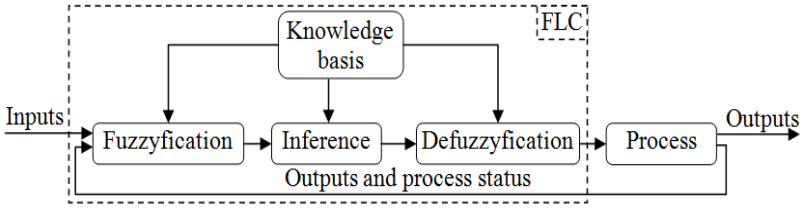

Fig.3.1 Fuzzy logic controller scheme and the controlled process.

Fuzzyfication can be defined as the mapping of the space into fuzzy sets.

By means of inference mechanism, that is a deductive process, the control goal can be derived.

The fuzzyfication and the inference work on the elements of the knowledge basis given by:

- A database (or dictionary) defining, through the associated membership functions, the fuzzy sets of each involved quantity. It translates numerical values into linguistic variables, making a partition, through fuzzy sets, of the universe of the speech. Better resolutions can be achieved increasing the number of the terms, but with an increase

of complexity. One peculiarity of the fuzzy systems is the possibility that an element of the universe can belong to various sets: this allows distributing the possible decisions among various classes of inputs, increasing the system robustness.

- A rules base, i.e. the selection of the fuzzy rules. These rules represent the control actions as they create a correlation among the fuzzy sets defined in the database.

Defuzzyfication is a mapping from a space of fuzzy control to a space of non-fuzzy (crisp) control action. The defuzzyfication mechanism leads to a numerical output from the result of the inference.

3.3. FUZZY LOGIC REVIEW.

This section summarized some of the basic concepts of fuzzy set theory and fuzzy logic with a special emphasis to their use in a fuzzy logic controller design. [4]-[5]

3.3.1. Fuzzy Set.

Let *U* be a set, called the universe of discourse, and let *u* be the generic element of *U.*

Definition 1: A fuzzy set *B* in an universe of discourse *U* is characterized by a membership function μ_B which takes values in the interval [0,1], i.e. $\mu_B : U \rightarrow [0,1]$.

Therefore, a fuzzy set *B* in *U* may be represented by an ordered pairs collection of a generic element *u* and its grade of membership function $\mu_B(u)$: $B = \{(u, \mu_B(u) \mid u \in U\}$.

When *U* is continuous, the notation is:

$$B = \int_U \mu_b(u)/u \tag{3.1}$$

When U is discrete, the notation is:

$$\sum_{i=1}^{n} \mu_B(u_i)/u_i \tag{3.2}$$

Definition 2: The set of all points *u* in *U* such that $\mu_B(u)>0$ is called the support of a fuzzy set *B*.

In particular, fuzzy singleton is a fuzzy set whose support is a single point in *U*.

3.3.2. Fuzzy Set Operation.

The possible operation are reviewed in Fig 3.2

Definition 3: Union.

The membership function $\mu_{A\cup B}$ of two fuzzy sets union is defined by:

$$\mu_{A\cup B}(u) = \max\{\mu_A(u), \mu_B(u)\} \tag{3.3}$$

Definition 4: Intersection.

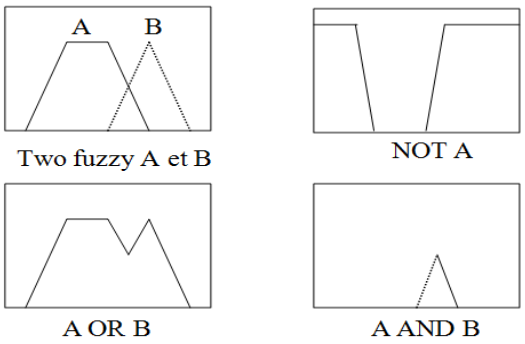

Fig.3.2 fuzzy operations on fuzzy sets.

The membership function $\mu_{A\cap B}$ of two fuzzy sets intersection is defined by:

$$\mu_{A\cap B}(u) = \min\{\mu_A(u), \mu_B(u)\} \tag{3.4}$$

Definition 5: Complement

The membership function $\mu_{\bar{A}}(u)$ of two fuzzy sets intersection is defined by:

$$\mu_{\bar{A}}(u) = 1 - \mu_A(u) \tag{3.5}$$

3.3.3. Linguistic Variable.

A linguistic variable is characterized by a quintuple (*x, T(x), U, G, M*) in which *x* is the name of variable; *T(x)* is the term set of *x* that is, the set of names of linguistic values of *x* with each value being a fuzzy number defined on *U*; *G* is a syntactic rule for generating the names of values of *x*; and *M* is a semantic rule for associating with each value its meaning. Each term of *T(x)* is characterized by a fuzzy set in the universe of discourse *U*. these terms can be characterized as fuzzy sets with the use of membership functions.

3.3.4. Fuzzy System.

To define a fuzzy system a definition of the fuzzy set should be done. A fuzzy membership function defines a fuzzy set because it gives the degree of membership of an element to that set.

In the following, some of the most used shapes for the membership functions will be reviewed.

- The triangular shape. This membership requires three parameters {*a, b, c*}:

$$\text{triangle}(\chi; a, b, c) = \max\left[\min\left(\frac{\chi - a}{b - a}, \frac{c - \chi}{c - b}\right), 0\right] \tag{3.6}$$

- The trapezoidal shape. This membership requires four parameters {*a, b, c, d*}:

$$trapezoid(\chi; a, b, c, d) = \max\left[\min\left(\frac{\chi - a}{b - a}, 1, \frac{d - \chi}{d - c}\right), 0\right] \tag{3.7}$$

Previous membership functions are the most used because they do not need hard mathematics to be defined and they could be easily implemented. However, other shapes with better performances in some special circumstances can be used. Some of them will be briefly reviewed.

- The Gaussian shape. This membership requires two parameters {σ, *c*}:

$$gaussian(\chi; \sigma, c) = e^{\{-[(\chi - c)/\sigma]^2\}} \tag{3.8}$$

Where *c* is the centre and σ is the basis of the Gaussian shape.

- The bell shape. This membership requires three parameters {*a, b, c*) Fig 3.3:

$$bell(\chi;a,b,c) = \frac{1}{1+\left|\frac{\chi-c}{a}\right|^{2b}} \tag{3.9}$$

Where *b* usually is positive.

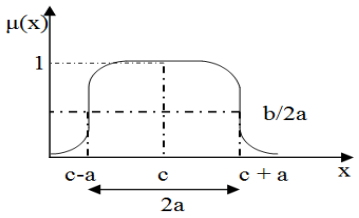

Fig.3.3 Bell shape.

- Moreover there is also the "singleton" shape that need only one parameter {*a*} :

$$\text{singleton}(\chi;a) = \begin{cases} 1....x = a \\ 0...x \neq a \end{cases} \tag{3.10}$$

The latter one represents a Boolean set, which can be considered as a particular case of a fuzzy set. In fact the singleton defines a set to which the element *x* could totally belong or not, thus with only two possible degree of membership 0 or 1. The importance of this type of fuzzy set (Fig 3.4) will be clear in the following pages where the implementation problem for a fuzzy logic based controller will be addressed.

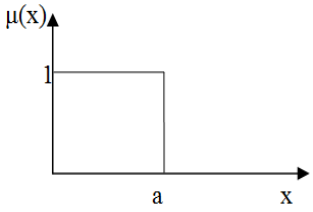

Fig.3.4 singleton shape.

Some membership functions shapes examples are shown in Fig 3.5

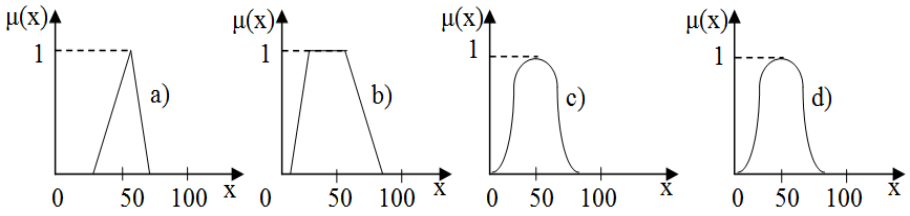

Fig.3.5 some membership functions examples:

a) triangle (x;20,60,80); b) trapezoid (x;10,20,60,90); c)Gaussian(x;100,50); d)bell(x;20,5,50).

3.3.5. Fuzzy Rule.

A fuzzy rule is a particular of two or more fuzzy set and it is the basis of the fuzzy inference mechanism through which the decisions are taken. One fuzzy rule IF-hen is like:

If χ is *A* then *y* is *B*

"χ is *A*" is called "antecedent" while "*y* is *B*" is called "consequent". *A* and *B* are fuzzy sets defined in *X* and *Y*.

It has been shown that a fuzzy set can be defined by a fuzzy membership function: χ and *y* belong to *A* and *B* not completely but partially, thus a certain degree of membership for both of them can be defined. Moreover, one rule is a binary relation R defined in the *X* x *Y* space. In conclusion also to R is associated a degree of membership to the *X* x *Y* space, identified by $\mu_R(\chi,y)$.

There are two possible interpretations of a fuzzy rule:

a) $A \Rightarrow B$ means "A linked to B" equivalent to:

$$R = A \Rightarrow B = AxB = \int_{XxY} \mu_A(\chi) \tilde{*} \mu_A(y)/(\chi, y) \tag{3.11}$$

Where * means AND fuzzy.

b) $A \Rightarrow B$ means "A implies B" equivalent to this operation:

$$R = A \Rightarrow B = -A \cup B \tag{3.12}$$

In the following, only the interpretation a) will be used. In Fig 3.6 the interpretations are shown. With reference to the first one, a fuzzy rule is seen as a patch that covers a group of x and y values rather than one *x* value and one *y* value. From this, it is clear the possibility of a fuzzy rule to model unclear situations.

3.3.6. Fuzzy Inference Process.

Once introduced the fuzzy sets, the membership functions, and the fuzzy rule, the explanation of the inference process is straightforward. The inference process is the heart of the fuzzy logic because it allows its generalization. Starting from an assumption and a rule that is not valid for the same assumption but for similar one, the fuzzy inference gets to a conclusion near to the conclusion stated by the rule.

This can be theoretically described by the definition 6.

Definition 6: *A* and *A'* are fuzzy sets of *X* with $A' \subset A$ and B fuzzy set of Y. $A \Rightarrow B$ is a fuzzy rule *R* on *XxY*. Then the fuzzy set *B'* result of "χ is A' " and by the rule "if χ is *A* then *y* is *B*" is defined by:

$$B' = \{(y, \mu_B(y)) | y \in Y\} \tag{3.13}$$

On the other hand, by:

$$B' = A' \circ R = A' \circ (A \Rightarrow B) \tag{3.14}$$

With

$$\mu_{B'} = \max_x \min[\mu_{A'}(\chi), \mu_R(\chi, y)] \triangleq \vee_\chi [\mu_{A'}(\chi) \wedge \mu_R(\chi, y)] \tag{3.15}$$

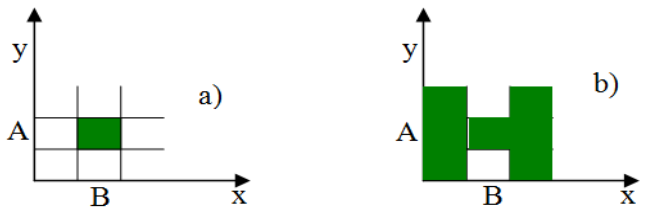

Fig 3.6 Interpretations of fuzzy rule.

"χ *is A'* " is the assumption that combined with a rule like "if χ is *A* then y is *B*" gives a conclusion that is based on the assumption, on the rule and on the relation of *A'* with *A* and so is a generalization of the rule.

The inference process is (in the fuzzy theory) something like function *f(x)* is in the traditional mathematics. This analogy is evident from Fig 3.7.

If *A* is a fuzzy set defined on *X* and *F* one relation on *XxY*, to find the resulting set *B*, one should build the cylindrical extension of *A*, *c(A)*, then the intersection of *c(A)* and *F* gives the analogous of I (Fig 3.7); considering the projection of $c(A) \cap F$ on *Y*, *B* comes out.

Considering μ_A, $\mu_{c(A)}$ and μF the degrees of membership of the fuzzy sets *A*, c(A) and *F* with $\mu_{c(A)}(\chi, y) = \mu_A(\chi)$,then:

$$\mu_{[c(A)\cap F]} = \min\left[\mu_{c(A)}(\chi, y), \mu_F(\chi, y)\right] = \min\left[\mu_A(\chi), \mu_F(\chi, y)\right] \tag{3.16}$$

Projecting c(A)∩F on Y:

$$\mu_B = \max_x \min\left[\mu_A(\chi), \mu_F(\chi, y)\right] \hat{=} \vee_x \left[\mu_A(\chi) \wedge \mu_F(\chi, y)\right] \tag{3.17}$$

(3.17) is called max-min composition and indicated with $B = A \circ F$.

If one choose the product for the fuzzy AND, and the max for the fuzzy OR the max-product composition is obtained:

$$\mu_B \hat{=} \mathrm{V}_x\left[\mu_A(\chi).\mu_F(\chi, y)\right] \tag{3.18}$$

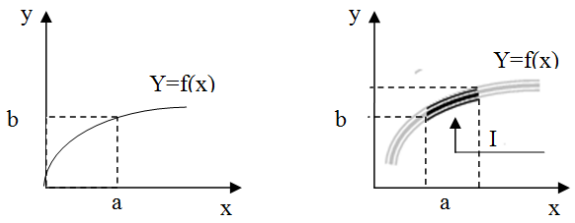

Fig 3.7 The inference is a generalization of the function concept from traditional mathematics

The fuzzy sets could be used both in the antecedent and in the consequent ("Mamdani style") or only in the antecedent, using in the consequent a mathematical function ("Sugeno style"). It is clear that a fuzzy controller should have as output a number not a fuzzy set.

Thus, it could be helpful to use Sugeno style in the inference process to avoid that stage called defuzzyfication used to obtain a crisp value from fuzzy output. Moreover, if the consequent uses a fuzzy singleton, the style is Mamdani but it can be seen also like a Sugeno with a simple mathematical function (the constant). With this option, the defuzzyfication process is considerable easier and it needs reduced computational resources.

In the following different inference example ("Mamdani style") employing a different number of rules and of antecedents will be reviewed.

3.3.6.1. One rule with one antecedent.

This situation is described by Fig 3.8:

"If χ is *A* then z is *B*" and χ is *A*'. Thus the set B' is defined by:

$$\mu_{B'} = \vee_x \left[\mu_{A'}(\chi) \wedge \mu_A(\chi)\right] \wedge \mu_B(y) = \omega \wedge \mu_B(y) \tag{3.19}$$

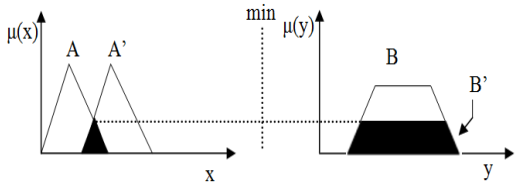

Fig 3.8 One rule and one antecedent.

The interpretation of the Fig 3.8 example is easy: the intersection of *A'* and *A* determines how much is true the rule if instead of "*x* is *A*" the antecedent was "*x* is *A'* "

3.3.6.2. One rule with two antecedents.

This situation is described by Fig 3.9:

"if χ is *A* and *y* is *B* then *z* is *C*" with χ is *A'* and *y* is *B'*.

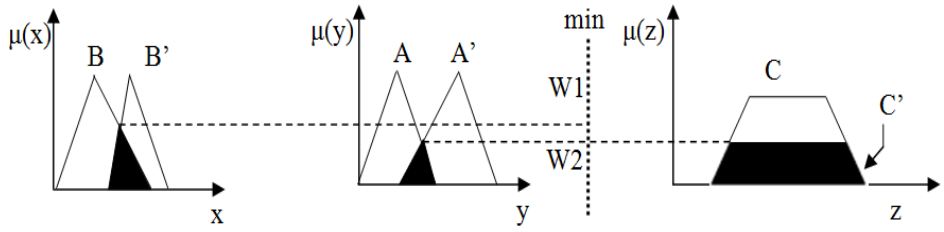

Fig 3.9 One rule and two antecedents

Let us consider this more complex situation gradually:

1. assumption "χ is *A*" and "*y* is *B*"
2. rule "if χ is *A* and *y* is *B* then z is *C*"(*AxB*⇒*C*)
3. conclusion "z is C"

The rule is defined by the following factor:

$$\mu_R(\chi, y, z) = \mu_{(AxB)xC}(\chi, y, z) = \mu_A(\chi) \wedge \mu_B(y) \wedge \mu_C(z) \tag{3.20}$$

C' is defined as:

$$C' = (A' x B') \circ (AxB \Rightarrow C)$$

Thus:

$$\begin{aligned} \mu_{C'}(z) &= \vee_{x,y} \{[\mu_{A'}(\chi) \wedge \mu_{B'}(y)] \wedge [\mu_A(\chi) \wedge \mu_B(y) \wedge \mu_C(z)]\} \\ &= \vee_{x,y} \{[\mu_{A'}(\chi) \wedge \mu_{B'}(y) \wedge \mu_A(\chi) \wedge \mu_B(y)]\} \wedge \mu_C(z) \\ &= \underbrace{\{\vee_x [\mu_{A'}(\chi) \wedge \mu_A(y)]\}}_{\omega_1} \wedge \underbrace{\{\vee_y [\mu_{B'}(y) \wedge \mu_B(y)]\}}_{\omega_2} \wedge \mu_C(z) \\ &= \omega_1 \wedge \omega_2 \wedge \mu_C(z) \end{aligned} \tag{3.21}$$

Where:

ω_1 expresses the relation between *A* and *A'*

ω_2 expresses the relation between *B* and *B'*

$\omega_1 \wedge \omega_2$ is how much the rule is true.

Thus is the less true of the two antecedents to determine how much the rule is true: the use of the min operation for the fuzzy y AND leads to a conservative approach.

3.3.6.3.Multiple rules with multiple antecedents.

This situation is described by Fig 3.10

"if χ is *A1* and *B1* then z is *C1*"and "if χ is *A2* and *y* is *B2* then z is *C2*" with χ is *A'* and y is *B'*.

Let us follow a step-by-step analysis:

Assumptions "χ is *A'* "and "*y* is *B'* "

Rule 1 "if χ is *A1* and *B1* then z is *C1" (A1 x B1* $\Rightarrow$ *C1)*

Rule 2: "if χ is *A2* and *y* is *B2* then z is *C2" (A2 x B2*$\Rightarrow$ *C2)*

Conclusion "z is C' ", defined by

$$C' = (A' x B') \circ (R_1 \cup R_2) = \left[(A' x B') \circ R_1\right] \cup \left[(A' x B') \circ R_2\right] \tag{3.22}$$

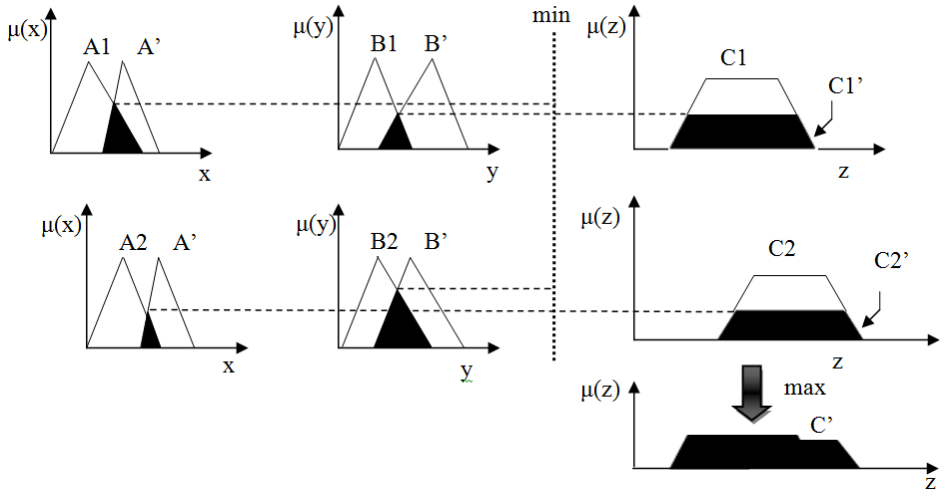

Fig 3.10 Two rules and two antecedents

3.3.7. FLC step-by-step Design Procedure.

The design of the controller is the result of the following procedure:

1 Identification of the characteristic quantities of the control. The characteristic advantage of the FLC is in the possibility to use all the information available and not only the error respect to the reference, used by PI-based control. If the control action should change for different working conditions, it is worth individuating, which parameters indicate in which state system is and which control action should perform.

2 Choice of the linguistic labels used in order to classify the measured values of each parameter and, when possible, identification of the range for each label. The FLC is based on the fuzzy definition of the parameters, thus it is crucial to define the fuzzy sets that can be used and the first step is to find their range.

3 Determination of the membership functions. After the choice of the labels and the definition of their allowable range have been done, then the membership function profiles must be designed. This step defines the fuzzy sets involved in the controller. Thus, once the involved parameters and their possible definition (fuzzy set) are chosen the framework of the controller can be defined even if the control action has not yet been chosen.

4 Writing of the rules of the controller. They are of the type: IF $\chi = A$ THEN $y = B$ and express the control action.

5 Transformation of the rules in codified expressions. It has been demonstrated in section 3.1, that the rules are the expression of operations on fuzzy sets. Thus the rule should be rewritten highlighting these operations.

6 Programming of the inference. The following procedure is executed by the controller:

   a. Determination of the degrees of the membership of the inputs.

   b. Check of the rules, through the evaluation of the degree of the antecedent part. If it is close to zero the rule is not “fired” i.e. it will not take part of the control action definition.

c. Attribution of the degree of the antecedent part to the consequent one. This means that the degree of validity of the rule, i.e. how much weight it will have in the control output, is determined by how much is true the antecedent.

7 Determination of the output of the control with the defuzzyfication process.

3.3.8. Implementation of the FLC.

There are two ways for a digital implementation of a fuzzy logic controller:

1. On–line implementation of the fuzzy algorithm. During each sampling period the microprocessor:

   1) Evaluates the degree of membership to the fuzzy sets of the inputs. For this step the " if then" loops are used thus several mathematical operations are needed;

   2) Weights the rules. For this step "min" and "max" operations are used;

   3) Determines the control output through defuzzyfication. For this step, several mathematical operations are used.

   The computational weight depends on the number of membership functions, on the number of the rules and on the chosen defuzzyfication method. The memory resources needed to store the program are not too large. The real limit of this kind of approach is the need for a high-speed microprocessor or DSP to execute the operation during each sampling period: this could be too high especially if the process to control has fast time constants.

2. Off–line implementation of the fuzzy algorithm: the overall program is prevently executed off – line for some discretized values of the inputs designing a look – up table, which will perform the actual control action. In this case huge memory resources could be needed in order to obtain a good control action. It is possible to use two distinct look – up tables one for fast tracking and the other for precise convergence. Otherwise, interpolation algorithms can be used too.

The first approach seems to be more interesting thanks to the possibility of the full exploitation of the fuzzy possibility that will be lost with a discretization of the control action. Moreover the price of fast microprocessors and DSP is rapidly decreasing. Let us have a brief overview of a fuzzy algorithm design.

3.3.8.1 Fuzzyfication

The first step is the Fuzzyfication. It is strongly influenced by:

1. The choice of the membership functions;
2. Their shape;
3. Their position in the input's range;
4. Their number.

The use of too high number of membership functions could lead to confusion in the action design. Especially in the control of power electronics process, in which the plant of the system under design has not a high order and fuzzy logic is used in order to optimize the control law and to take into account unmodelled non – linearities. On the contrary, the use of too few membership functions leads to a poor control action. Moreover, membership functions are overlapped (otherwise the fuzzy mechanism is not well exploited) but no more than two of them are overlapped at the same time. If the control law is decided by too many rules, it could be unclear and give unexpected results.

So let us assume that two membership functions are overlapped for each point. Thus with a IF THEN loop it is possible to define the range of the input and which membership functions will be fired. If the chosen membership functions are triangular, the degree of membership is simply determined by a linear function; in other cases the previously defined functions should be implemented leading to longer computation. Moreover even if triangular membership functions are adopted, if the slopes are different the number of ranges increases.

Let us consider the example in Fig 3.11 in the case b there are more ranges and for each of them the degree of membership should be independently determined. In the case a, instead, there are few ranges and the degree of membership to the two functions involved does not depend on the range. Clearly, the designer should weight the performances improvement possible with a different shape and adopt only the necessary asymmetries.

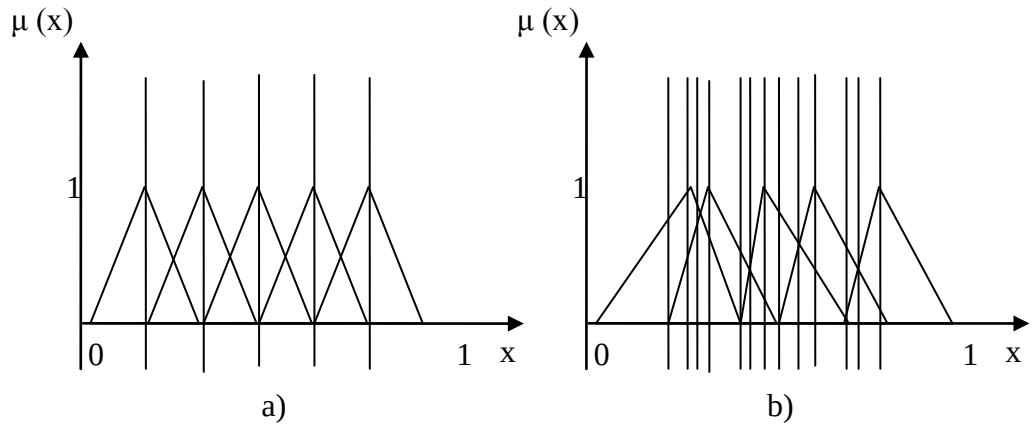

Fig 3.11 Two possible shaping of the same number of triangular membership functions.

3.3.8.2 Rules and defuzzyfication .

Once written the Fuzzyfication process, then the rules connect the input membership functions with the output ones and only min/max operations are needed.

The defuzzyfication process mainly depends on the adopted technique and on the shape of the output functions. In addition, in this case a good designer should make a trade – off between complexity and possible increase of the performances.

A commonly used defuzzyfication strategy is the so-called "centre of gravity". For discrete universe, the crisp control value is obtained by:

$$z_0 = \frac{\sum_{j=1}^{n} \mu(w_j) w_j}{\sum_{j=1}^{n} \mu_z(w_j)} \tag{3.23}$$

Where n is the number of quantization levels of the output.

The COG method is not only defuzzyfication method available as the Fig. 3.12 shows. However offers high performance at the price of higher computation complexity.

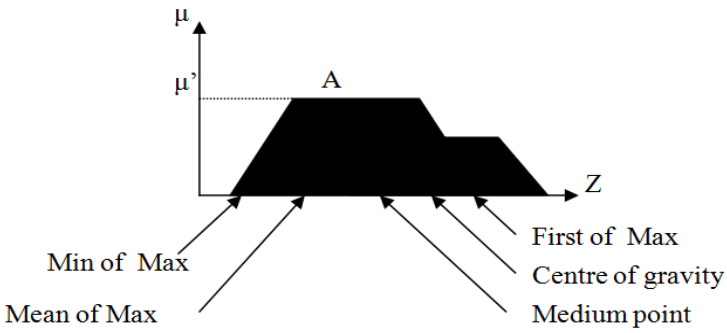

Fig 3.12 Different defuzzyfication strategies

Let us take a look to a simple to better understand how to write a FLC program.

First one has to define the input and output range ([-1 1]), the membership functions number (e.g. 3 for each variable) and shape (e.g. triangular for the input and singleton for the output) Fig 3.13. Then, the desired control action is defined through the rules reported in table 3.1.

The program can be further reduced due to system symmetry; on the contrary, each asymmetry makes the program longer increasing its execution time.

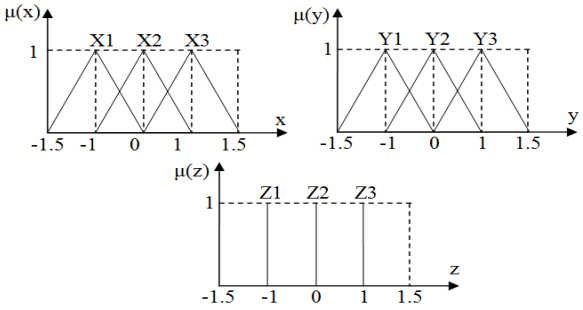

Fig 3.13 Membership functions for the inputs x and y and for the output z.

Table 3.1

FUZZY RULES

	X1	X2	X3
Y1	Z2	Z1	Z3
Y2	Z1	Z2	Z1
Y3	Z3	Z1	Z2

3.4. REVIEW OF THE TESTED APPLICATIONS OF THE FLC AT POWER CONVERTERS

The tested application of the fuzzy logic control that will be reported is in the field of AC/DC converter. The adopted scheme is a PI-type fuzzy controller. A fuzzy proportional controller and a fuzzy incremental one make the controller. The advantage of the use of the FLC over a traditional PI is the possibility of changing the control action on the basis of the different working condition. However, this kind of approach is limited by the PI structure.

The fuzzy logic controlled dc/dc boost converter discussed in the following has been designed as a part of the power-conditioning unit of a PFC system. The goal of this choice is to reduce complexity and costs increasing robustness and reliability. An uncontrolled diode rectifier, a fuzzy logic controlled boost converter and load, compose the power conditioning system. The simple power electronic structure, together with the fuzzy logic-based controller action, allow to obtain optimum results both in the load side current and voltage regulations and maximum power flow even under strongly variable load conditions.

The control of boost converter can be obtained managing the energy stored in its inductance and capacitance. A fuzzy logic controller is used to achieve a good and quit simple regulation not only of the output voltage but also of the inductor current. The inductor current reference signal, depending on the operating point, is computed by means of a low pass filter (Fig 3.14) in the assumption that the converter according to a power balance condition automatically adjusts the dc component of the current.

A mathematical model of the boost converter, useful for analyzing the dynamic behavior of the system, and a suitable representation of the load are required. Usually in the most part of the switching converter applications (low power systems such as domestic electronics equipment), a simple resistor is used to model the converter load.

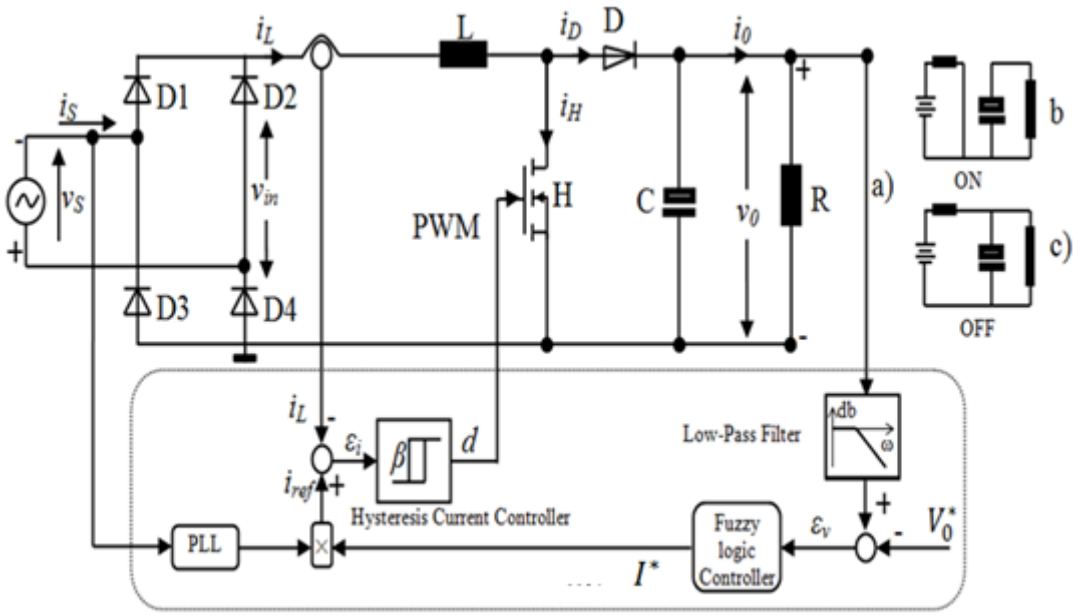

Fig 3.14 Fuzzy control scheme of AC-DC converter

Fig 3.14 presents the use of fuzzy logic to derive a practical control scheme for boost rectifier with active power factor correction. The methodology integrates fuzzy logic control technique in the feedback path and linear programming rule on controlling the duty cycle of the switch for shaping the input current waveform. The proposed approach avoids complexities associated with nonlinear mathematical modeling of switching converters. The control action is primarily derived from a set of linguistic rule written in accordance to experience and intuitive reasoning. Instead of generating fast pulse-width, modulated (PWM) signal. Computer simulations of the closed-loop performance in respect of load regulation and line regulation are presented and favorably compared to the ones obtained by the Peak current mode controller using small-signal modeling design technique.

The converter is described by the two following systems of differential equations depending on the states of the power device.

When H is ON

$$\frac{di_L}{dt} = \frac{v_{in}}{L} \tag{3.24}$$

$$v_0 = -\frac{1}{C}\int i_0 dt \tag{3.25}$$

When H is OFF:

$$\frac{di_L}{dt} = \frac{1}{L}(v_{in} - v_0) \tag{3.26}$$

$$v_0 = -\frac{1}{C}\int i_c dt = \frac{1}{C}\int (i_L - i_0)dt \tag{3.27}$$

The output signal of this fuzzy controller determines a suitable duty cycle during each operative condition.

Since the early 1970s, many small-signal modeling, analysis, and control techniques [1]-[4] for pulse-width modulated (PWM) switching converters have been proposed. Among various approaches, the most common ones are the averaging technique and its variants. Starting from the state space descriptions of the switched-mode converter for each circuit topology and using small-ripple approximations, an averaged linear time-invariant model is derived to replace a time-varying circuit. Then, the average signals are perturbed and neglecting second or higher order terms linearize the equations obtained. After separating the ac and dc parts, the s-domain transfer functions are found. The methodology is simple and elegant, and allows for the derivation of closed-form analytical expressions of the transfer functions. However, the model becomes inapplicable when the operating point of the converter is changed, such as a large-signal change in the input voltage and output load. Thus, the validity of these methods is restricted to small signal low-frequency application, and a major drawback would be the very limited range of fluctuation of system variables around the nominal operating point. In order to retrieve more useful information about the system, it is crucial that the model retains as many of the nonlinear properties of the physical system as possible. Recent research has been directed at applying nonlinear control principles to the dynamic control of converters. Many articles [5]-[7] for dc-dc converters address performance and design issues of using fuzzy logic to perform nonlinear control of the switching action. No exact models of converters are required or are important, and the system is controlled by fuzzy control algorithm, in which a set of

linguistic rules written in accordance to experience and intuitive reasoning. However, if the control methodology is directly applied to classical ac-dc converters with active power factor correction (APFC) [8], it might impose considerable computation time to deal with the fast-varying current loop. This part presents the use of fuzzy logic to derive a control scheme for boost rectifier with APFC. The methodology integrates fuzzy logic control technique in the feedback path and linear programming rule to control the duty cycle of the switch for shaping the input current waveform. The proposed approach avoids complexities associated with nonlinear mathematical modeling of switching converters. The control action is primarily derived from a set of linguistic rule written in accordance to experience and intuitive reasoning. Instead of generating fast-changing PWM signal.

3.5. FUZZY LOGIC CONTROLLER FOR BOOST RECTIFIER

The control action in a fuzzy logic controller is determined by a set of linguistic rules. Although it is necessary to have a thorough understanding of the converter to be controlled, it does not require a detailed mathematical model of the whole system. Fuzzy logic control has been investigated for applications such as motor drives and dc-dc converters; available literature on fuzzy control of APFC is limited. Objectives include tight output voltage regulation, high rejection of input voltage variations and load transients. Fig.3.17 shows the block diagram of the proposed fuzzy logic control scheme of the boost rectifier with APFC. The dc-bus voltage v_0 is scaled and is sampled by the digital apparatus and compared with a reference value V_0^*. The obtained error $\varepsilon_v(k)= V_0^*(k) - v_0(k)$ and its incremental variation $c\varepsilon_v(k)=\varepsilon_v(k)-\varepsilon_v(k-1)$ at the *kth* sampling instant are used as inputs for fuzzy controller. The output of the fuzzy algorithm is the variation magnitude of reference current δI^*. The dc-bus voltage is controlled by adjusting the magnitude of reference current I^*.

Where ρ and σ are constants, which are used to normalize the error and the change of error. The FLC consists of three major components [13], including Fuzzyfication, the action to the converter Decision-Making, and the Defuzzyfication. They are described as below.

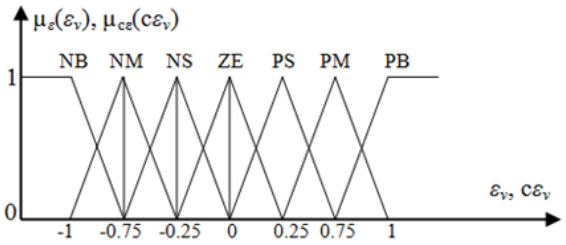

Fig. 3. 15 Membership functions adopted in the FLC

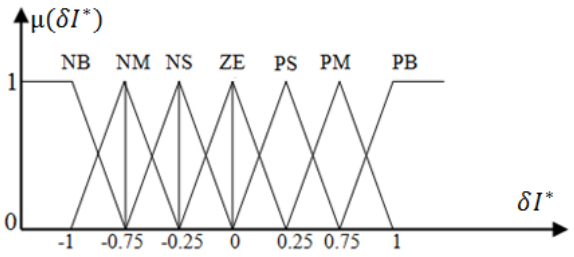

Fig. 3.16 Membership functions for δI^*.

3.5.1. Fuzzyfication.

Fuzzyfication is to map ε_v and cε_v in (Fig. 3.15) into suitable linguistic values. Seven fuzzy levels are defined for ε_v and cε_v**,** including negative big (NB), negative medium (NM), negative small (NS), zero ***(ZE),*** positive small (PS), positive medium (PM), and positive big (PB). Each input variable is assigned a membership value μ to each fuzzy set, based on a corresponding membership function. The number of fuzzy levels is not fixed and depends on the input resolution of needed. The larger the number of fuzzy levels, the higher is the input resolution. Fig. 3.15 shows the membership functions, which are triangular fuzzy-set values.

3.5.2. Decision-Making.

Decision-Making infers fuzzy control action from knowledge of the fuzzy rules and the linguistic variable definition. The control rules that determined the output of the FLC are based on the general knowledge of the system behavior or intuition of the process being controlled. As every ε_v and cε_v belongs to at most two fuzzy sets (Fig.3.15), a maximum of four rules have to be considered at every sample. Numerically, Table 3.2 shows the control rule table for the rectifier. The entries of the table are the normalized singleton values of the change of $\delta I^*(k)$. The inference result of the ith rule consists of two parts, including the weighting factor ω_i of the ith rule and the degree of change of $\delta I^*(k)C_i$, which is extracted from the control rule table 3.2. The

inferred output z_i of each rule is obtained by Mamdani's min fuzzy implication [13]. The inferred output of each rule is written as:

$$z_i=\min\{\mu_\varepsilon(\varepsilon_v), \mu_{c\varepsilon}(c\varepsilon_v)\}C_i =\omega_i C_i, \text{ i=1 to 4} \tag{3.28}$$

Where z_i is the calculated fuzzy representation of change in the control voltage inferred by the ith rule. Since the inferred output is a linguistic result, a defuzzyfication operation is carried out in the next operation in order to give the control action to the converter.

Table 3.2

Control rule table of the FLC

		Error (ε_v)						
		NB	NM	NS	ZE	PS	PM	PB
Change of error ($c\varepsilon_v$)	NB	NB	NB	NB	NB	NM	NS	ZE
	NM	NB	NB	NB	NM	NS	ZE	PS
	NS	NB	NB	NM	NS	ZE	PS	PM
	ZE	NB	NM	NS	ZE	PS	PM	PB
	PS	NM	NS	ZE	PS	PM	PB	PB
	PM	NS	ZE	PS	PM	PB	PB	PB
	PB	ZE	PS	PM	PB	PB	PB	PB

3.5.3. Defuzzyfication.

Defuzzyfication is to convert the inferred fuzzy control action to a non-fuzzy control action. The output of the FLC is the current command change of $\delta I^*(k)$ in (3.29) [i.e., $\delta I^*(k)$], which is integrated at regular *k*th sampling intervals and yields the following current command**.** The actual $\delta I^*(k)$ is determined by adding $\delta I^*(k-1)$to the calculated change,

$$I^*(k) = I^*(k-1) + \delta I^*(k) \tag{3.29}$$

During this operation, a crisp value for $\delta I^*(k)$ is calculated by using the center of gravity method. z_i and ω_i give the contribution of ith inference results to the crisp value. The final value of $\delta I^*(k)$ is determined by

$$\delta I^*(k) = \frac{\sum_{i=1}^{4} z_i}{\sum_{i=1}^{4} \omega_i} \tag{3.30}$$

Although (3.30) requires involving numerical multiplication and division of variables, is not necessary to be calculated at every sample since it is usually a slow varying quantity. The calculated control current is then sent to the output to hysteresis element.

Equation (3.29) gives an integrating effect, which increases the system type and improves the steady-state error. Another gain G_0 can also be applied to the fuzzy logic output $\delta I^*(k)$ to improve the performance. At steady state, a rapid change of $\delta I^*(k)$, is not desired, so a smaller G_0 is preferred. During a transient period, it is desired that $\delta I^*(k)$, is large to ensure fast response, so G_0, is larger. In this implementation, a gain of 1 is applied to $\delta I^*(k)$, when ε_i is close to 0, and a gain of 2 is employed in other cases, Initial tests with a 1.71 A load showed steady-state oscillations or slow response. In order to enhance steady state and transient response, a gain was applied to the error and change in error inputs. Extensive tests showed that a gain of 0.30 for the error and a gain of 3.92 for the change in error eliminated steady-state oscillations and improved the transient response. The new value of the current reference command, is given by

$$I^*(k) = I^*(k-1) + G_0 \delta I^*(k) \tag{3.31}$$

However, when these gains are less than 1, they can introduce steady-state error that cannot be eliminated by the integrating process in (3.30). In order to eliminate the steady-state error introduced by scaling the fuzzy logic inputs (the error and change in error), the error is scaled and added to $\delta I^*(k)$, so the control effort $I^*(k)$can expressed as:

$$I^*(k) = I^*(k-1) + G_0 \delta I^*(k) + G_i \varepsilon_v(k) \tag{3.32}$$

Where G_0 is the gain *for* fuzzy logic output, and G_i is the gain for the error. The term $G_i \varepsilon_v(k)$ also introduces an integrating process, and can smooth the transient response. It also eliminates the steady-state error. Since its main role is to eliminate the steady-state error, G_i is small compared to G_0. In this implementation, G_i equals 0.27. Finally the fuzzy logic controller for the output loop then can be illustrated as Fig. 3.17

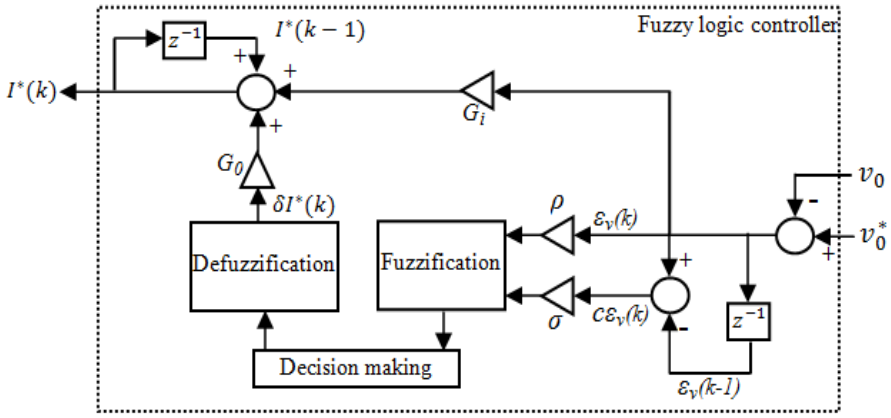

Fig. 3.17 Fuzzy logic controller for APFC.

3.6. SIMULATION RESULTS.

The power circuit is designed to meet the following specification:

Table 3.3

Design specification and circuit parameters.

Switching frequency	f_{sw}=20kHz
Output power	P_0=121W
AC amplitude of supply voltage	V_{SM}=150V
DC output voltage	V_0=160V
Input current ripple	≤2.5%
Output voltage ripple	≤2%
Load resistance	R=212Ω
Input Inductance	L=22.5mH
Output Capacity	C=940μF

The performance of the converter under steady state, large-signal output voltage and load change is investigated. Fig. 3.18 shows the steady state input voltage and current waveforms. It can be seen that the current is in phase with the voltage, showing unity power factor.

When the system has been entered into steady state, there is step change in the load R from 212 Ω to 312 Ω and from *312*Ω to *212* Ω with constant reference output voltage. The waveforms of the control voltage and the output voltage during transient period are shown in Fig. 3.19. After a short transient, the dc-bus voltage is maintained close to its reference value with a good

approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 3.4.

The dynamic behavior of the proposed fuzzy logic control under a step change of V^*_0 is presented in Fig. 3.20. After a short transient, the dc-bus voltage is maintained close to its new reference with good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 3.5

Fig. 3.21 shows the transient of the step change of v_s in the proposed fuzzy logic control by decreasing v_s from *150 V* to *140 V* and increasing them from *140 V* to *150 V*. After a short transient, the dc-bus voltage is maintained close to its new reference with good approximation and stability. The line currents have nearly sinusoidal waveforms. The corresponding transient values are shown in table 3.6.

Nevertheless, the input current is still sinusoidal during transient. It can be seen from the above that the system is stable during the large-signal change in the output voltage and the output load. Further research will be dedicated into the optimization of the fuzzy rules, in order to have further improvement in the transient behaviors.

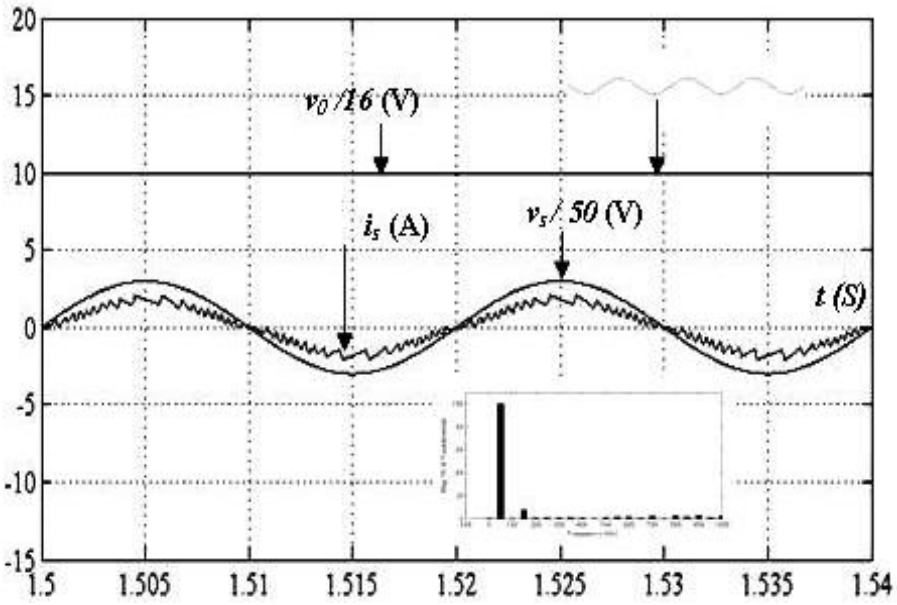

Fig 3.18 Simulated basic signal waveforms in steady state

under UPF, V^*_0*=160 V, THD=2.92%.*

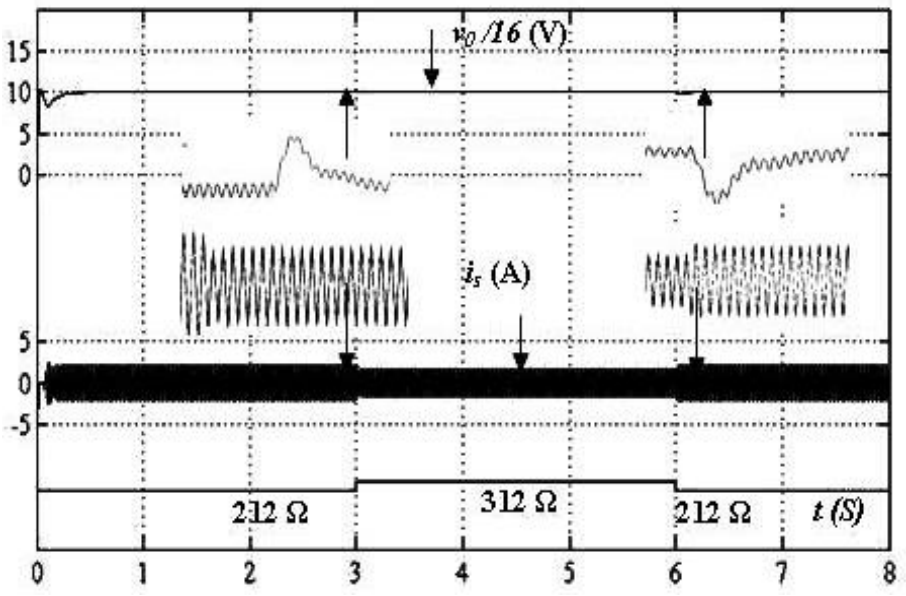

Fig.3.19 Transient of the step change of the load Increasing from *212*Ω to *312*Ω and Decreasing from *312* Ω to *212*Ω.

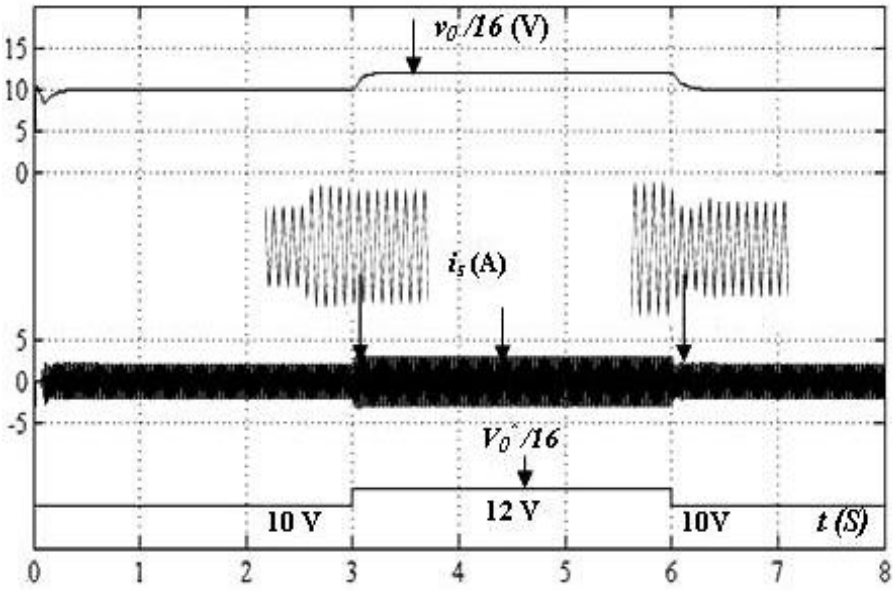

Fig.3.20 Transient of the step change of V^*_0, Increasing from *160 V* to *192 V* and Decreasing from *192 V* to *160 V*.

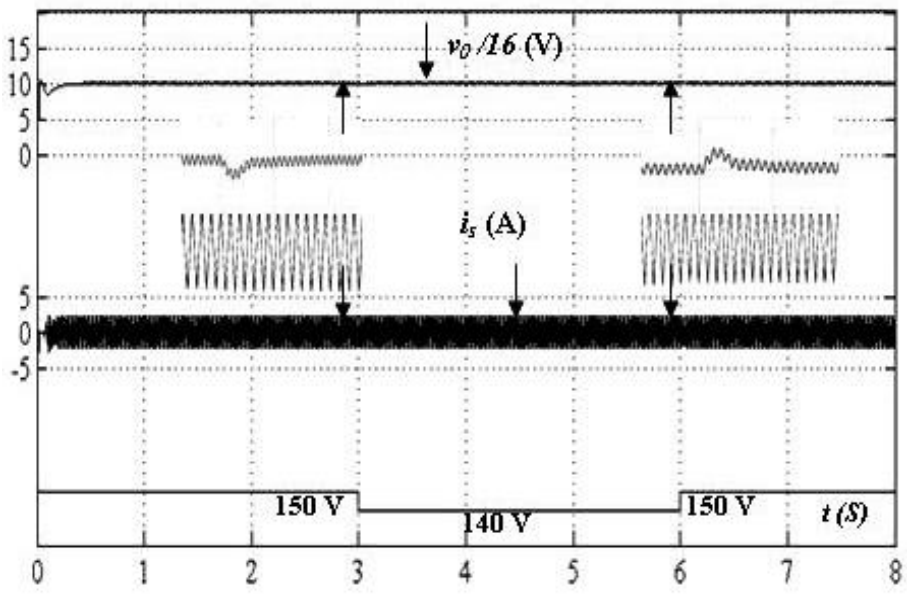

Fig. 3.21 Transient of the step change of v_s, decreasing from *150 V* to *140 V* and increasing from *140 V* to *150 V*.

Table 3.4

Transient values corresponding to Fig 3.19.

Load	ΔV_0 *(V)*	Δt *(S)*	ΔI_{ref} *(A)*	Δt *(S)*
212Ω/312Ω	*1.6*	*0.045*	*0.69*	*0.05*
312Ω/212Ω	*1.6*	*0.045*	*0.69*	*0.05*

Table 3.5

Transient values corresponding to Fig 3.20.

V^*_0	ΔV_0 *(V)*	Δt *(S)*	Δ*Iref (A)*	Δt *(S)*
160V/192V	*32*	*0.075*	*1.25*	*0.09*
192V/160V	*32*	*0.075*	*1.25*	*0.09*

Table 3.6

Transient values corresponding to Fig 3.21.

v_s	ΔV_0 *(V)*	Δt *(S)*	Δ*Iref (A)*	Δt *(S)*
150V/140V	*0.8*	*0.058*	*0.35*	*0.08*
140V/150V	*0.8*	*0.060*	*0.35*	*0.08*

3.7. CONCLUSION.

This chapter presents a fuzzy logic controller AC-DC boost rectifier with PFC. It integrates fuzzy logic control technique in the feedback path and linear programming rule on controlling the magnitude of the reference current, in order to adjust the duty cycle of the switch for the input current shaping. The proposed approach avoids complexities associated with non-linear mathematical modeling of switching converters. The control action is primarily derived from a set of linguistic rule written in accordance to experience and intuitive reasoning.

REFERENCES.

[1]. R.D. Middlebrook and S. Cuk, **"A general unified approach to modeling switching converter power stages,"** in Proc. IEEE Power Electron. Special. Conf. Rec., 1976, pp. 18-34.

[2]. F.C. Lee, R.A. Carter, "**Investigations of stability and dynamic performances of switching regulators employing current injected control,"** IEEE Trans. Aerospace and Electronic System, vol. 19, no. 2, pp. 274-287, Mar. 1983.

[3]. F. Ueno, T. Inoue, 1. Oota, and M. Sasaki, **"Regulation of Cuk converters using fuzzy controllers,"** in INTEL.EC '91 Record, 1991, pp. 261-267.

[4]. B. K. Bose, "**Expert system, fuzzy logic and neural network applications in power electronics and motion control,"** Proc. IEEE, vol. 82, no. 8, pp. 1303-1323, 1994.

[5]. W.C. *So,* C.K. Tse, and Y.S. Lee, **"Development of a fuzzy logic controller for dc/dc converters: design, computer simulation, and experimental evaluation,"** *IEEE Trans. Power Electron,* vol. I I, no. 1, pp. 24-31, Jan. 1996.

[6]. **Henry S.H. Chung, Eugene P.W. Tam, and S.Y .R. Hui, "Development of a Fuzzy Logic Controller for Boost Rectifier with Active Power Factor Correction,"** pp. 149-154, 1999 IEEE

[7]. T. Gupta, R.R. Boudreaux, R.M. Nelms, and J.Y. Hung, **"Implementation of a fuzzy controller for dc-dc controllers using an inexpensive 8-b microcontroller"** IEEE Trans. Ind. Electron., vol. 44, no. 5, pp. 661-669, Oct. 1997.

[8]. Dake He and R. M. Nelms, "**Fuzzy Logic Average Current-Mode Control for DC-DC Converters Using an Inexpensive 8-Bit Microprocessor,"** Proceedings of the 2004 39th lEEE Industry Applications Society (IAS 2004) Annual Meeting, Seattle, Washington, October 2004, pp. 2615-2622.

[9]. Dake He and R. Mark Nelms, **"Fuzzy Logic Peak Current-Mode Control for DC-DC Converters Using an Inexpensive %Bit Microcontroller,"** IEEE, pp. 2000-2006, 2005.

[10]. E. Vidal-Idiarte, L. Martinez-Salamero, F. Guinjoan, J. Calvente and S. Gomariz, **"Sliding and fuzzy control of a boost converter using an 8-bit microcontroller,"** IEE Proc.-Electr. Power Appl., Vol. 151, No. 1, pp. 5-11, January 2004.

[11]. A. Rubaai, M. F. Chouikha, **"Design and Analysis of Fuzzy Controllersfor DC-DC Converters"** in First International Symposium on Control, Communications and Signal Processing, 2004, pp. 479- 482.

[12]. A. Khoshooei, and 1. S. Moghani, **"Implementation of a Single Input Fuzzy Controller for a High Power Factor Boost Converter,"** in IEEE AFRICON, 7th Africon conference in Africa, Technology innovation, 2004, Gaborone, Botswana, pp. 69-72.

[13]. Fredy H. Martinez S, Diego F. Gomez M, "**Fuzzy Logic Controller for Boost Converter with Active Power Factor Correction,"** The 7th International Conference on Power Electronics. October 22-26, 2007 / EXCO, Daegu, Korea.

CONCLUSION.

In this study, we presented the command of AC-DC converters permitting to have a power factor near to the unit this strategy of command used is based on an adjustment by voltage loop corrector and current loop corrector.

Stricter requirements and harmful effects of distorted line current have prompted a need for power factor correction of converters. An additional power processing stage in a power supply increases the cost of the product. Low power supplies are, however, mass production devices, and are therefore sensitive to any additional increase in the manufacturing cost. in a single-stage converter only one active switching stage is used.

The simulation design constraints of power-factor-correction power supplies that use a cascading structure PI_PI, PI_ Hysteresis control and fuzzy_hysteresis control to achieve high power factor and fast regulation have been study. In addition, the small-signal model of the proposed converter was developed, from witch an optimal PI compensator is designed for the converter system with peak-current mode control. Therefore, comprehensive simulations studies were performed to capture the performance of the proposed controls for single-phase power factor correction. First, the steady-state performance is evaluated in terms of output voltage regulation, THD, and power factor.

Next, the transient performance is evaluated for output voltage response on application of load step changes, reference voltage step and the step change of v_s that are expected in practical applications of this circuit, after a short transient, the dc-bus voltage is maintained close to its reference value with a good approximation and stability. The line currents have nearly sinusoidal waveforms.

However, the input current harmonic content is very close to the limit. The static performances of the variable band hysteresis controller are compared to those of the Fixed band hysteresis controller. The results show that the VBH control has THD of the input current much better then with the fixed band hysteresis control, thus, the fuzzy logic control avoids complexities associated with non-linear mathematical modeling of switching converters. The control action is primarily derived from a set of linguistic rule written in accordance to experience and intuitive reasoning. Simulations results have been shown that fast dynamic response; good output regulation, and high power factor can be achieved with

the proposed single-stage converter and control scheme. By comparing the three controllers we find that, the fuzzy logic control active power correction is the better control while looking at the rapidity of the response time in the transient state and low harmonic distortion, with the proposed single-stage converter and control scheme.